

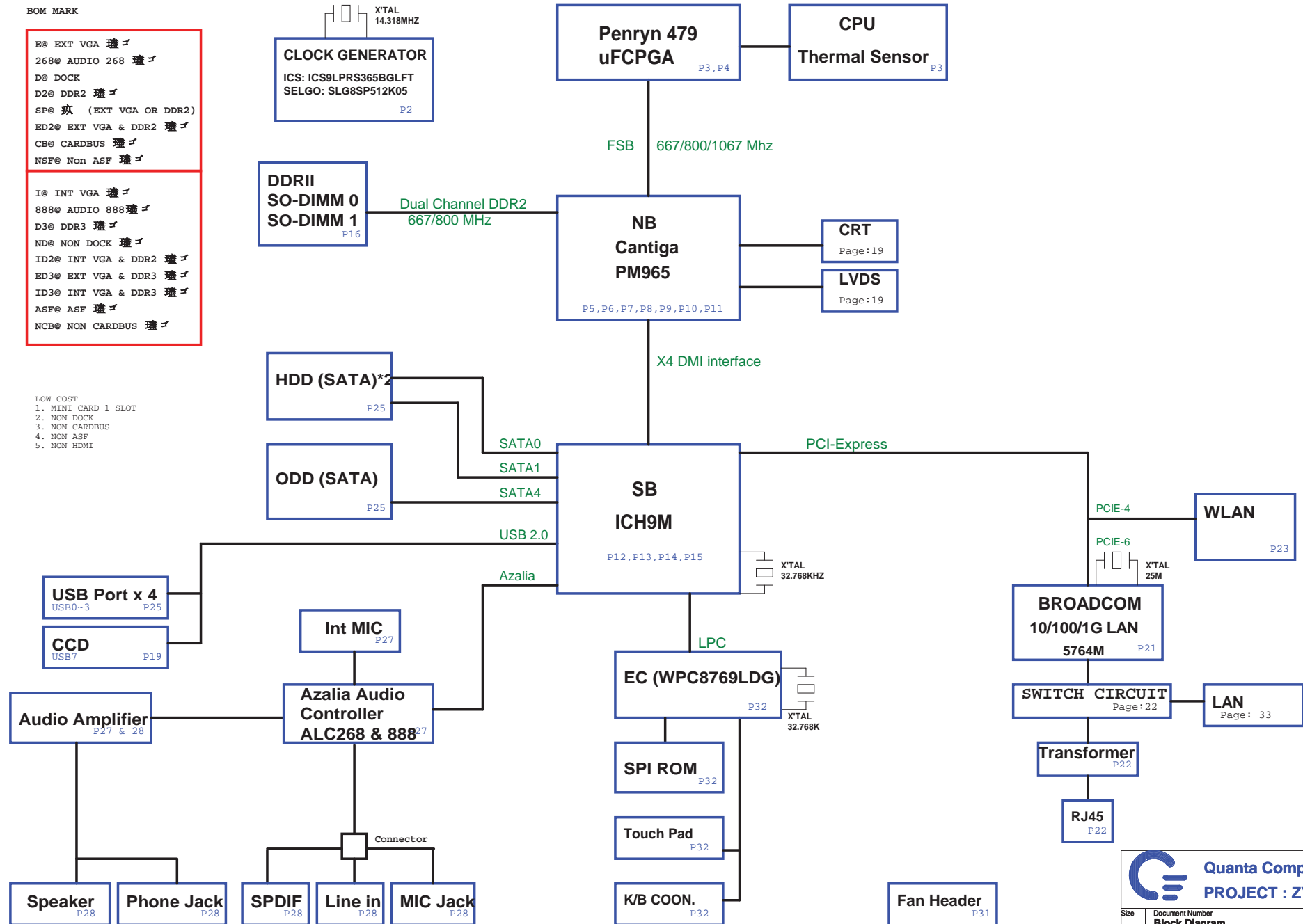
ZY6D SYSTEM BLOCK DIAGRAM

BOM MARK

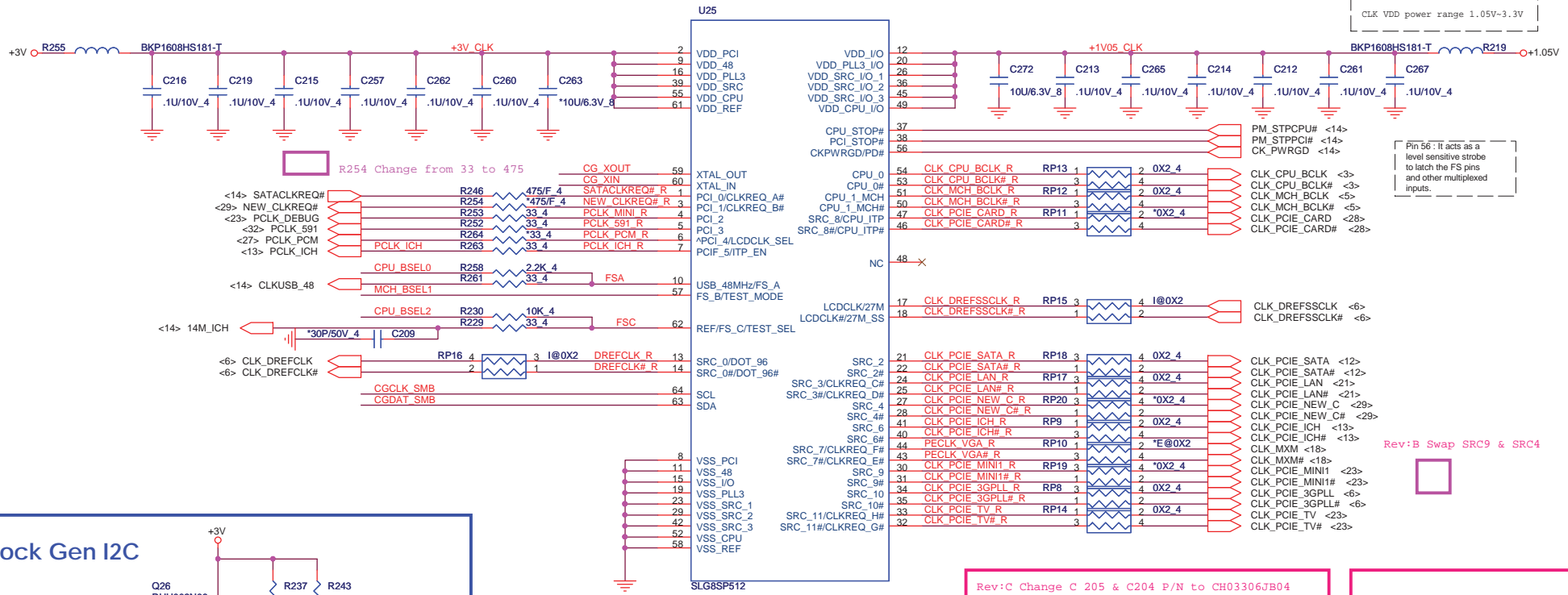
B@ EXT VGA 璫
 268@ AUDIO 268 璫
 D@ DOCK
 D2@ DDR2 璫
 SP@ 痾 (EXT VGA OR DDR2)
 ED2@ EXT VGA & DDR2 璫
 CB@ CARDBUS 璫
 NSF@ Non ASF 璫

I@ INT VGA 璫
 888@ AUDIO 888璫
 D3@ DDR3 璫
 ND@ NON DOCK 璫
 ID2@ INT VGA & DDR2 璫
 ED3@ EXT VGA & DDR3 璫
 ID3@ INT VGA & DDR3 璫
 ASF@ ASF 璫
 NCB@ NON CARDBUS 璫

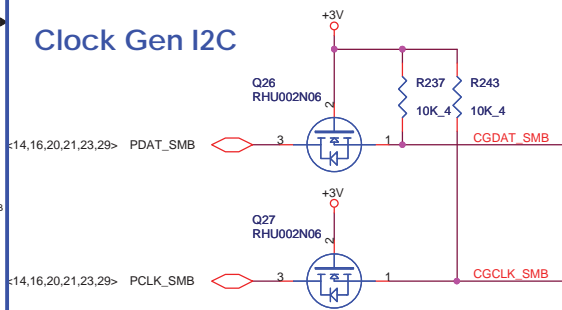
LOW COST
 1. MINI CARD 1 SLOT
 2. NON DOCK
 3. NON CARDBUS
 4. NON ASF
 5. NON HDMI



Clock Generator

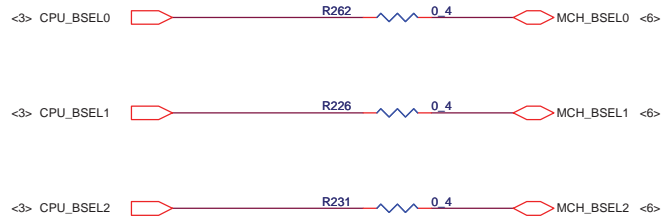


Clock Gen I2C



CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection

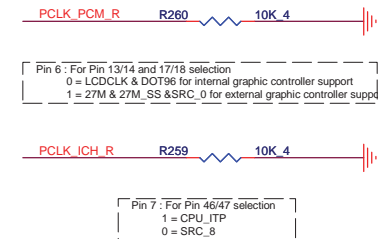


CRB Rev0.7 : 110(CBA)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

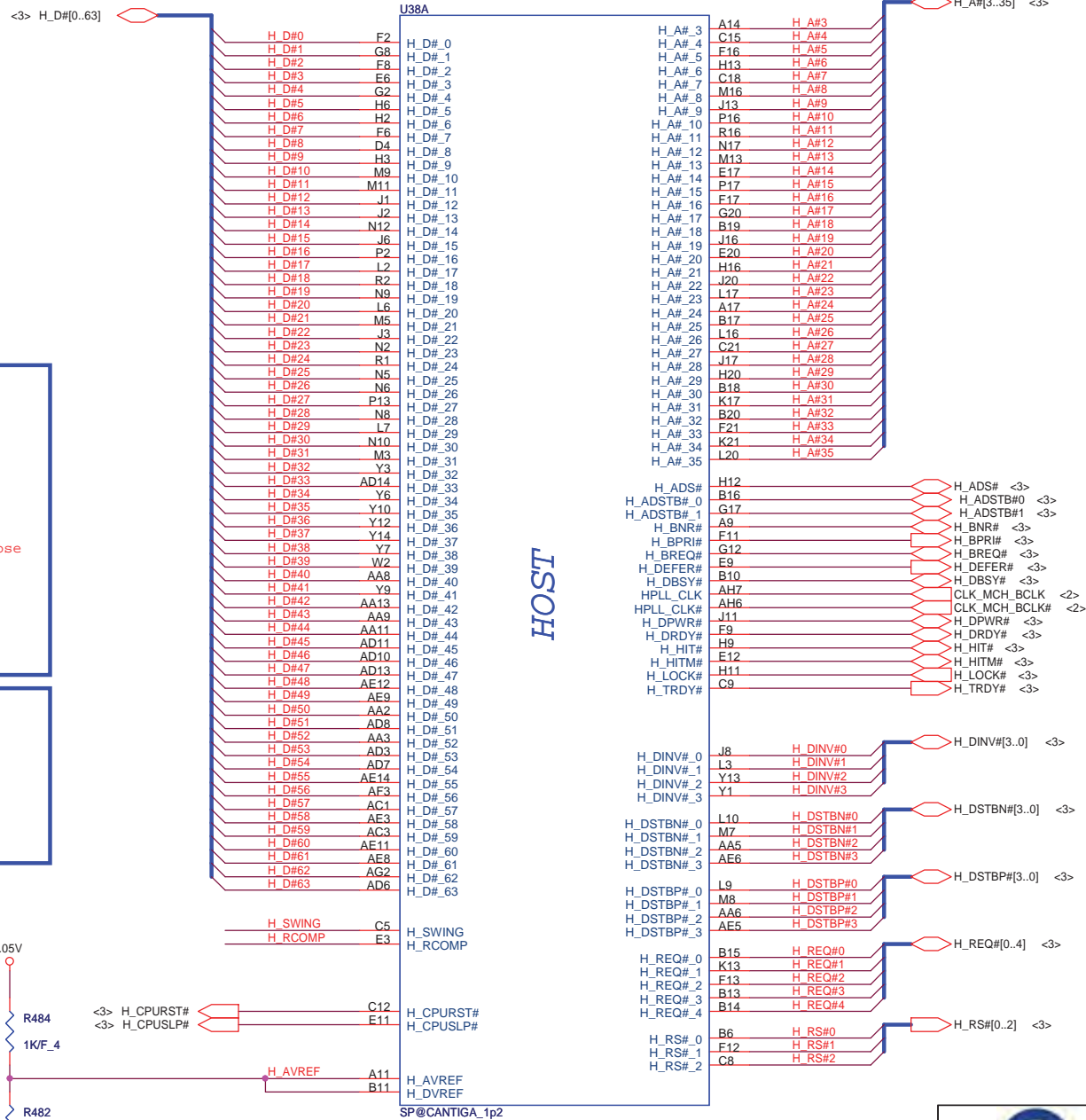
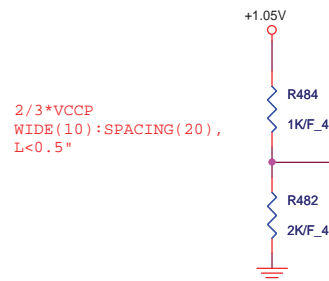
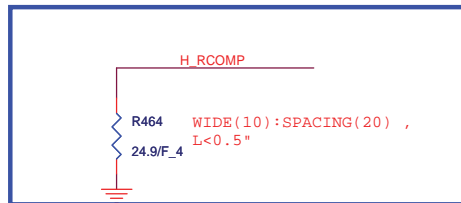
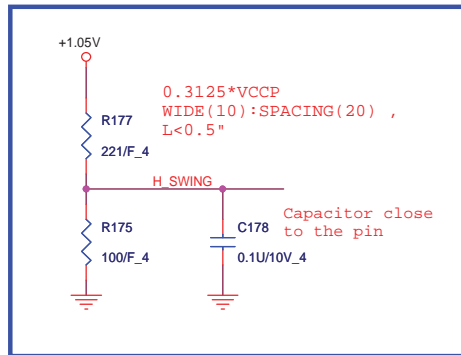


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
Date:	Thursday, August 26, 2008	Sheet 2 of 40

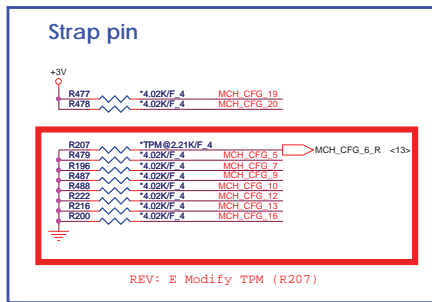


	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



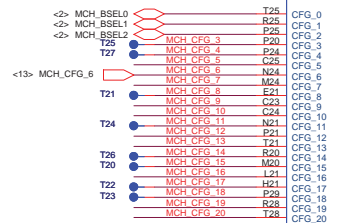
Strap table

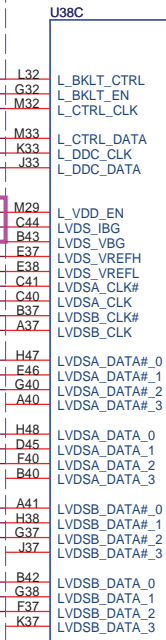
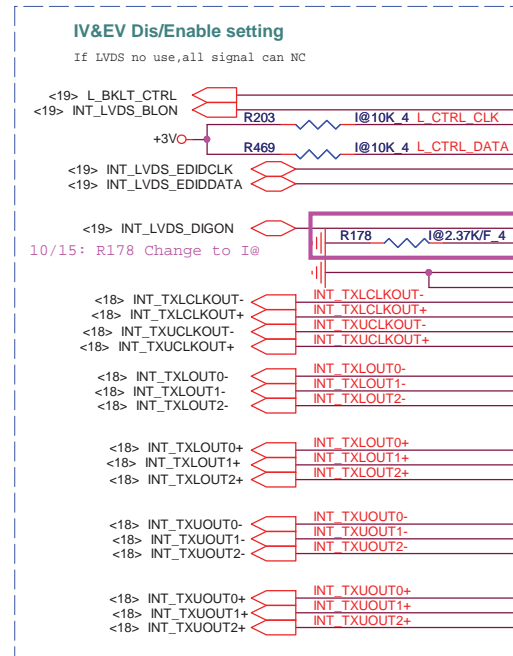
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	MS TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/HDMI) or PCIe is operational (Default) 1 = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via PEG port	0 = Only Digital Display port (SDVO/DP/HDMI) or PCIe is operational (Default) 1 = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present



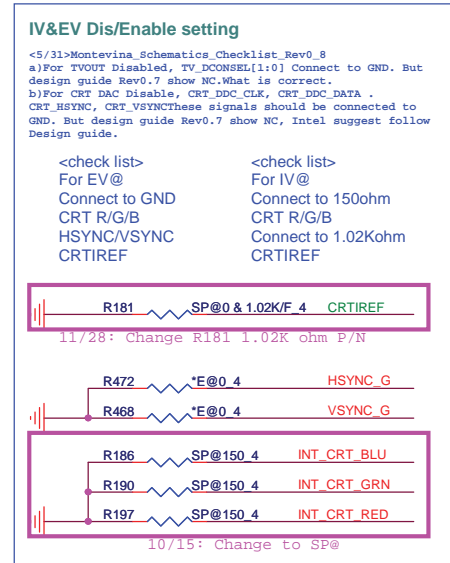
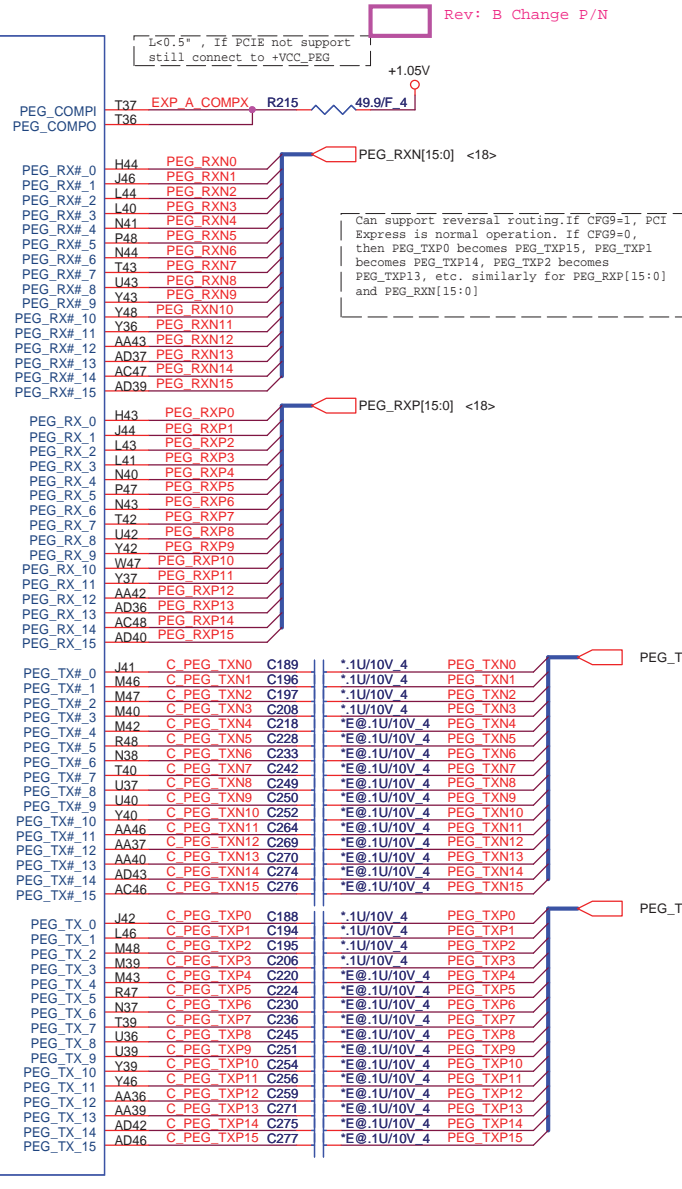
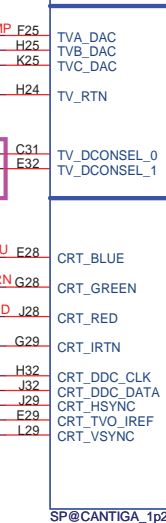
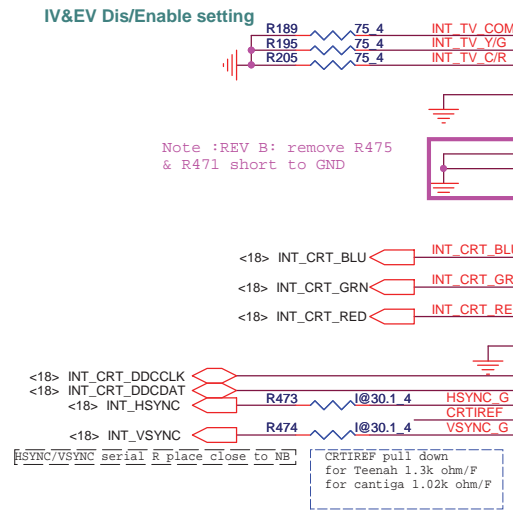
HB Thermal trip pin
No use Thermal trip HB side can
NC (HB has OUT)

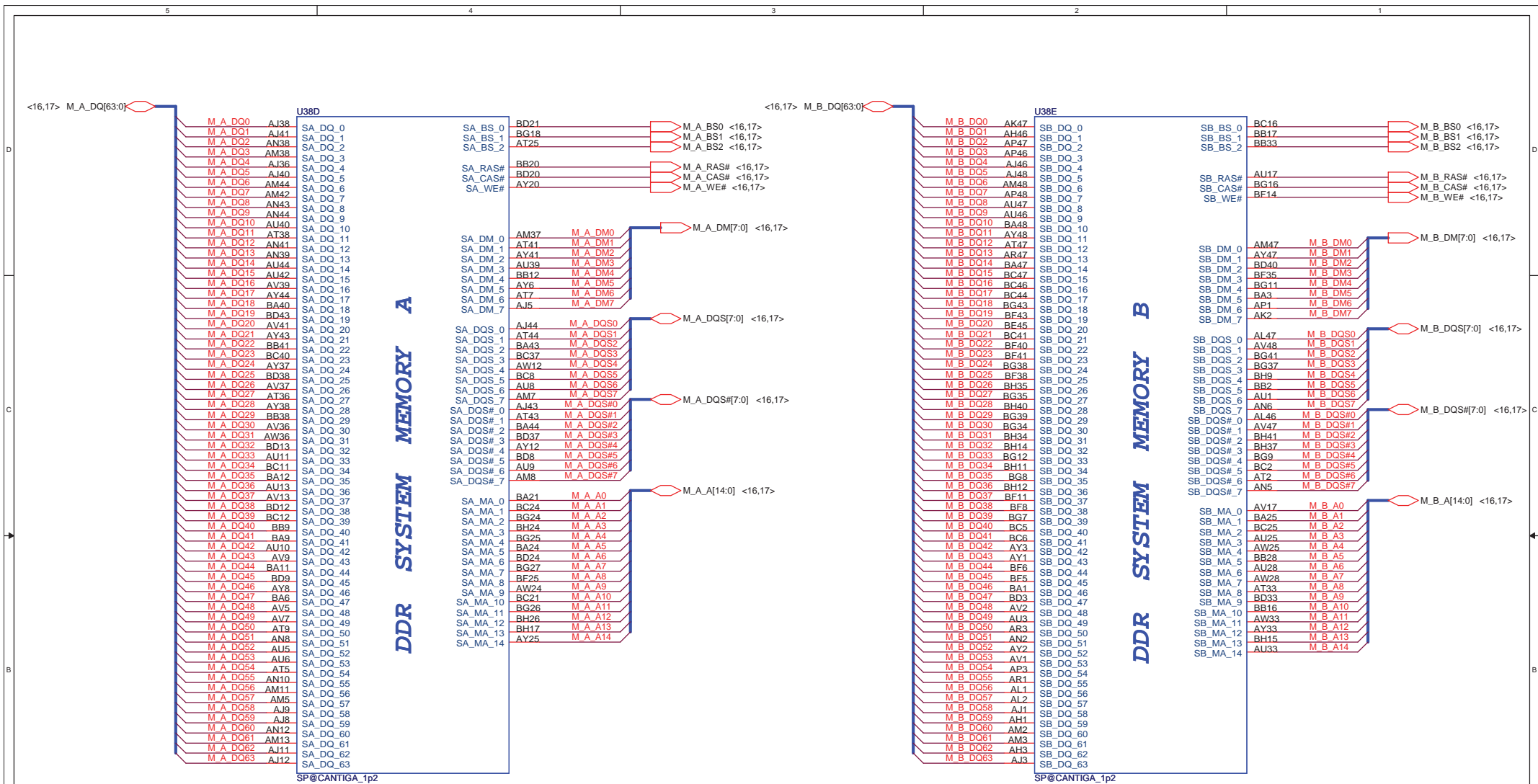
PM_DPSTP#
The Daisy chain topology should
be routed from ICH9M to IMVP,
then to (G)MCH and CPU, in that
order.





LVDS
A.I.
PCI-EXPRESS
VGA





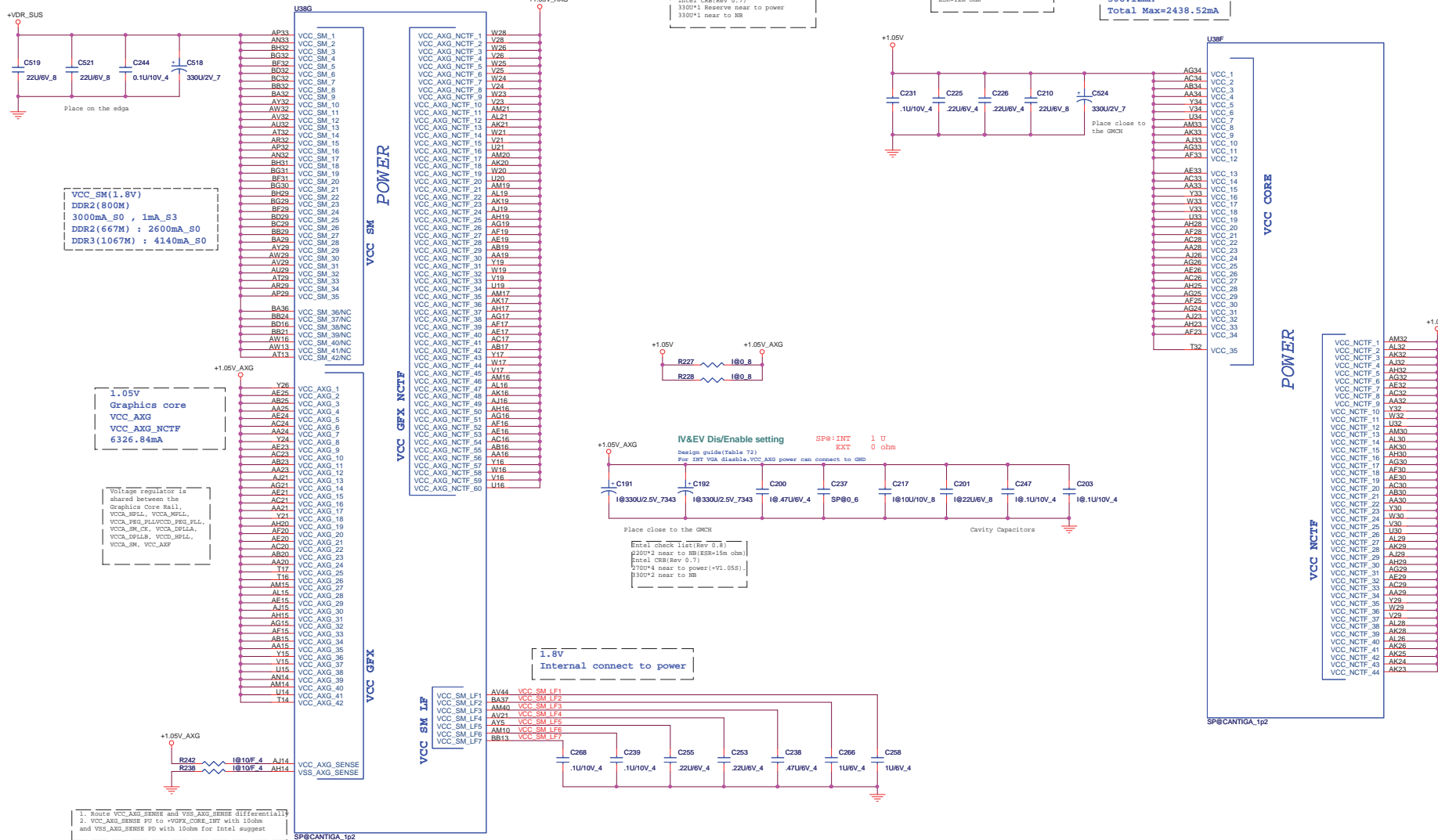
Power consumption reference to Intel
644135 Cantiga chipset EDS Volumel.
Section 10

GM TDP 10.5-12W
GS TDP 7-8W
PM TDP 7W

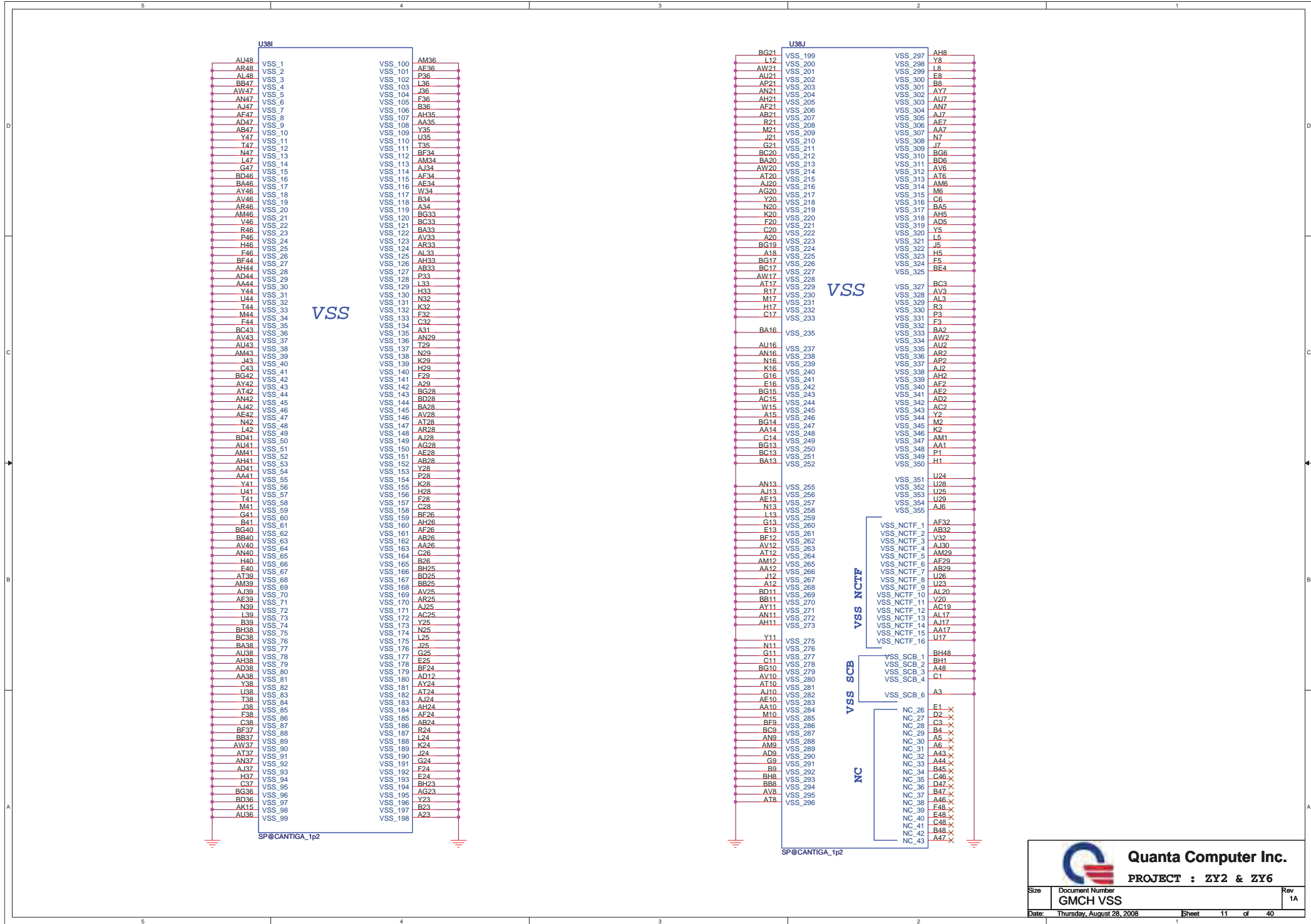
Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
3300*1 Reserve near to power
3300*1 near to NB

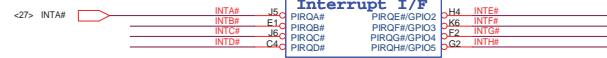
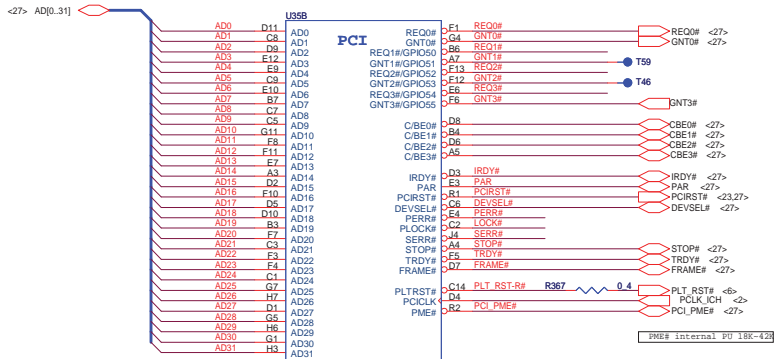
Intel check list(Rev 0.8)
2700*1 near to power(+V1.05M).
2700*2 near to NB
Intel CRB(Rev 0.7)
2700*1 near to power(+V1.05M).
2700*1 near to NB
ESB=12m ohm

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

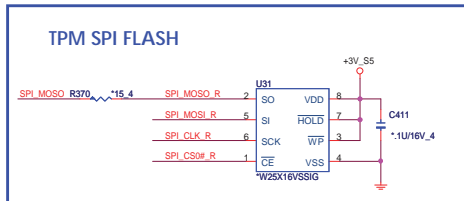
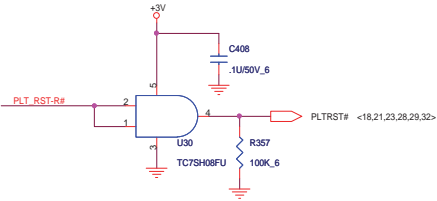






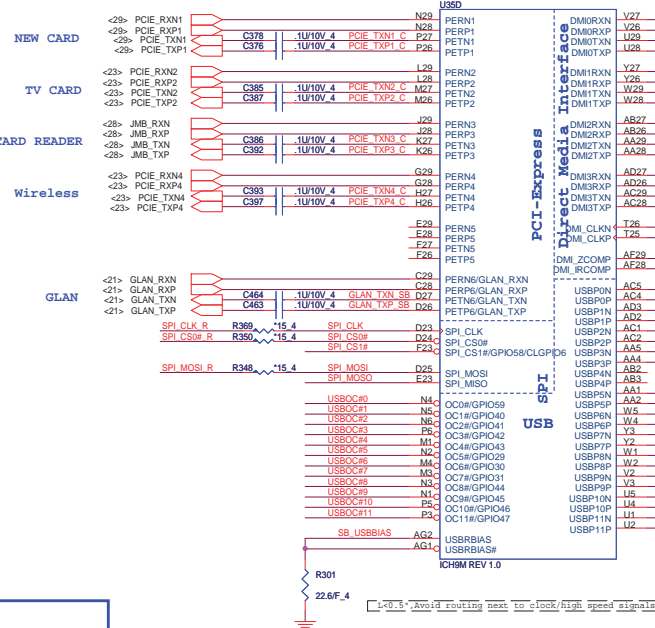


TM & AS	Y
LOW COST	N

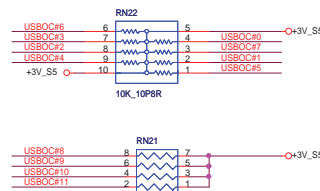
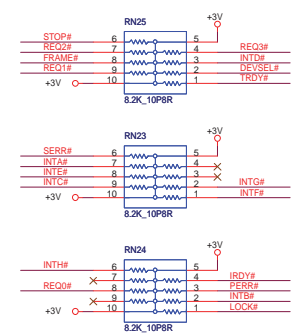
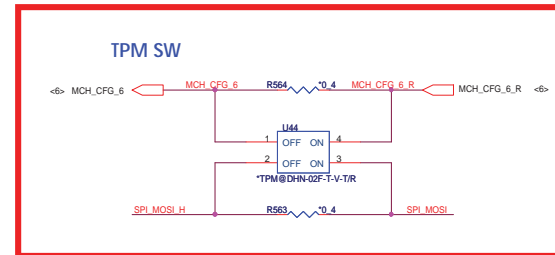


South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD		
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC	

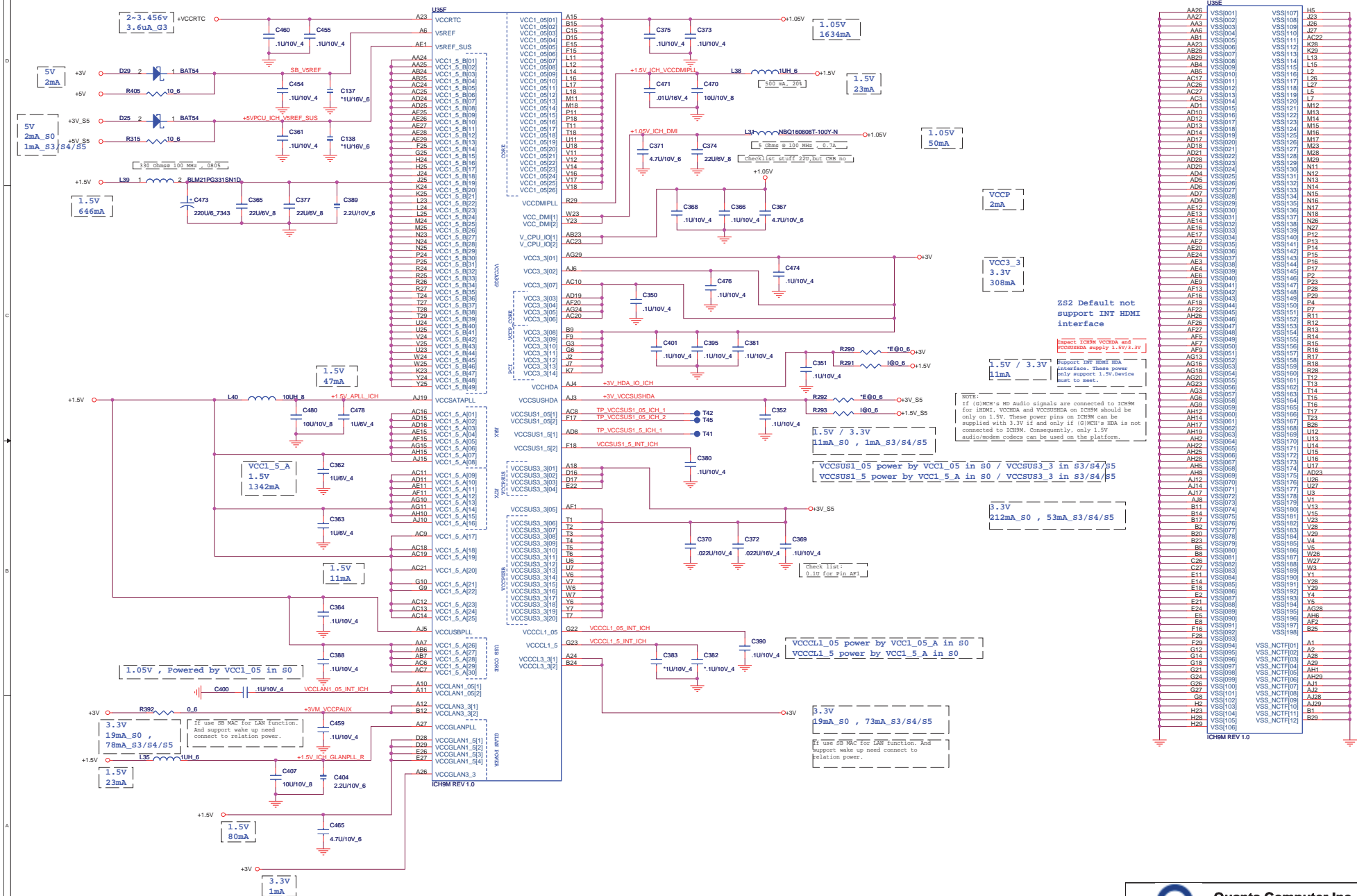


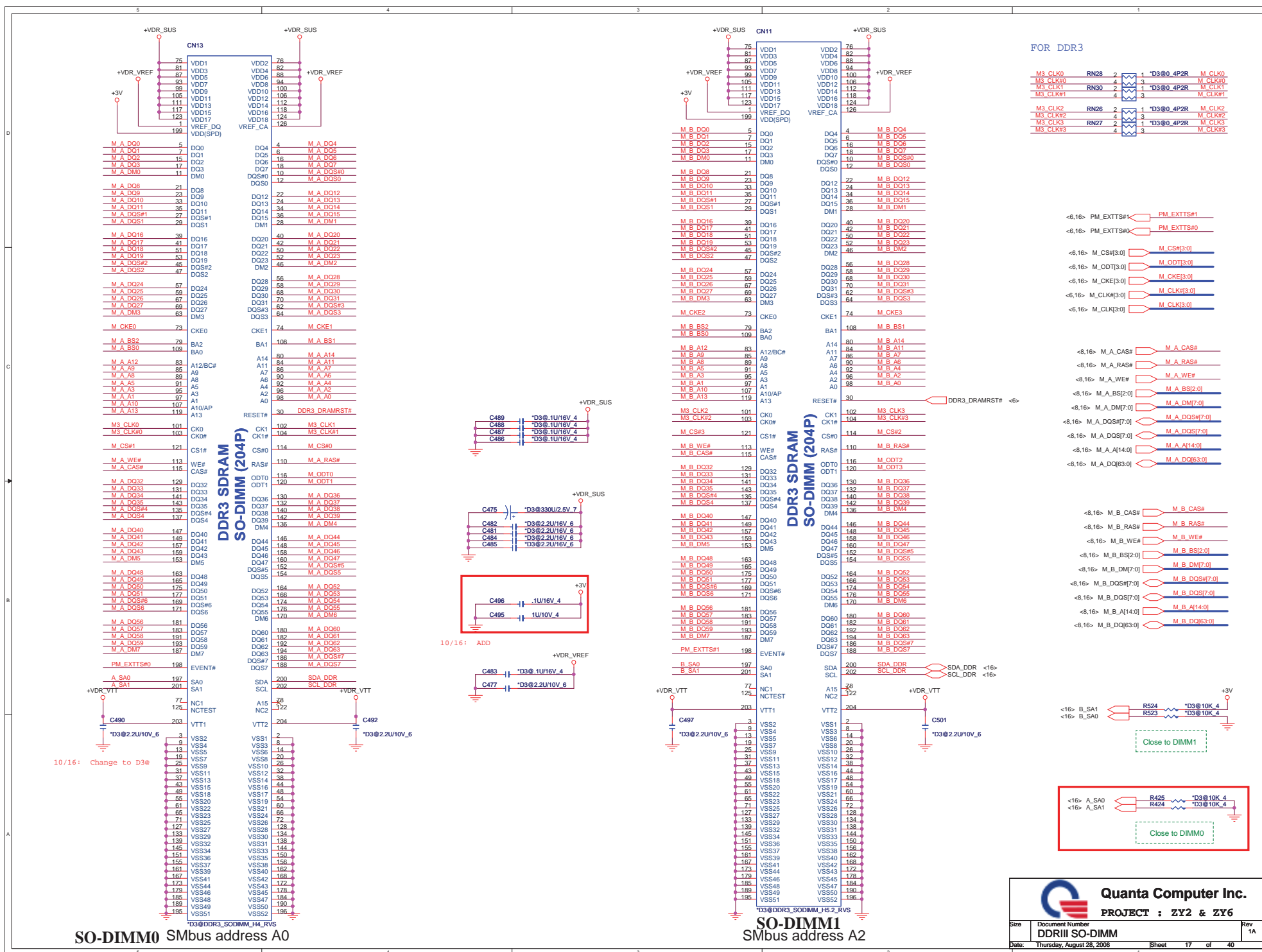
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	IC9M9M PCIE / PCI / USB	1A
Date	Thursday, August 28, 2008	Sheet 13 of 40

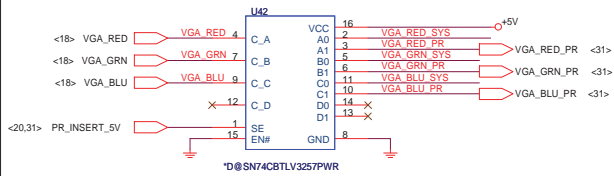




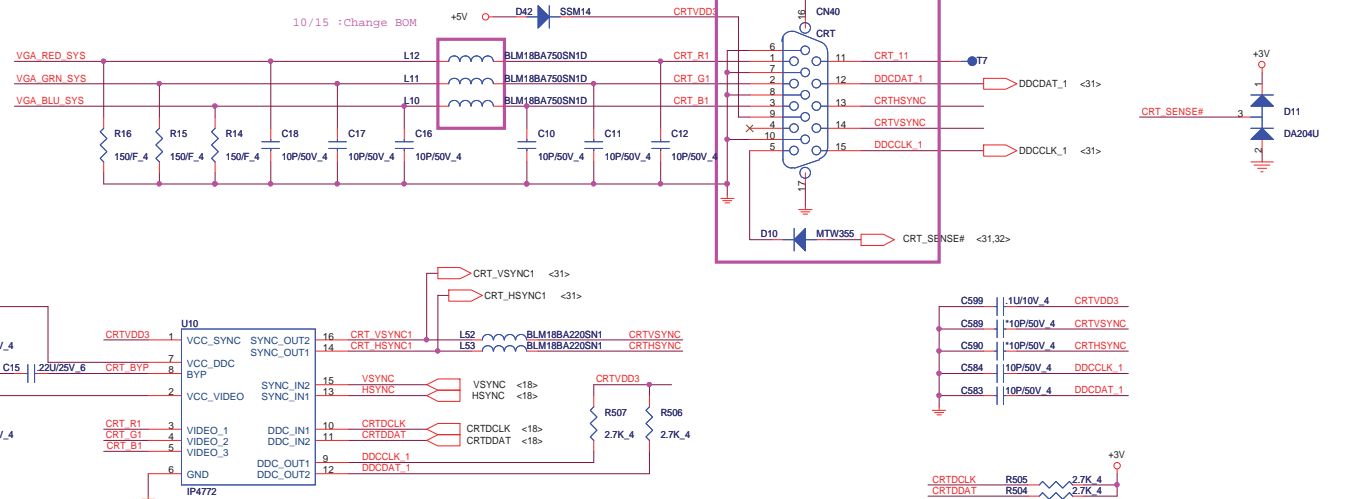


CRT Select

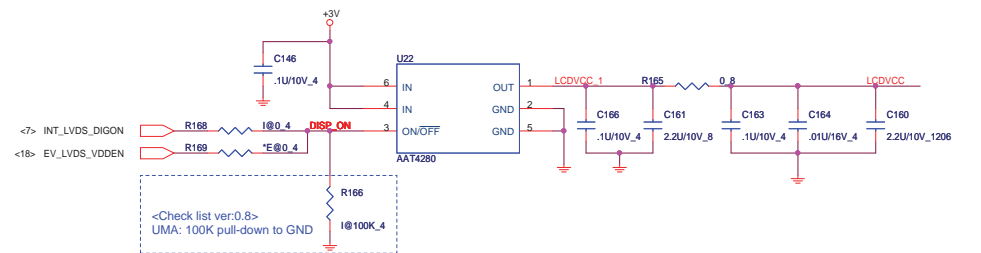
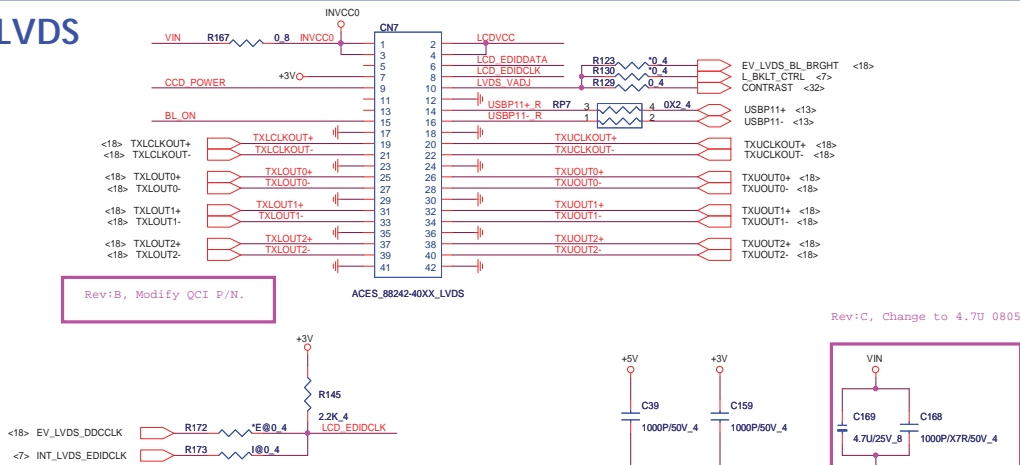
CRT SWITCH



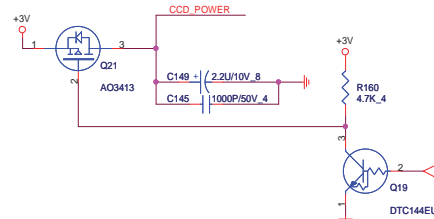
CRT CONNECTOR AND ESD



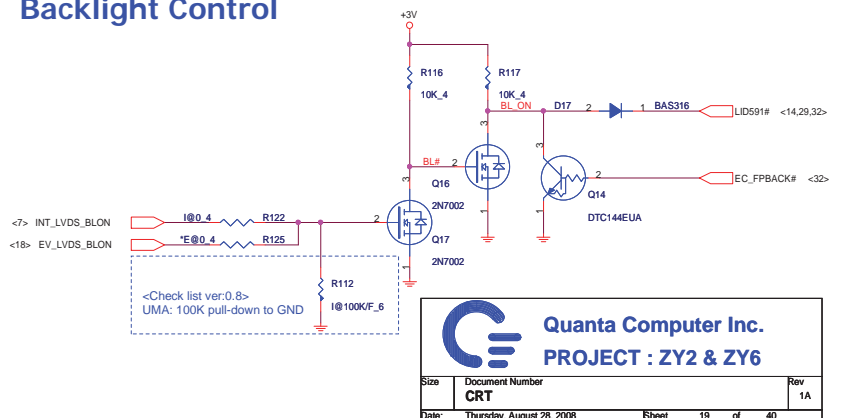
LVDS



CAMERA MODULE CONNECTOR

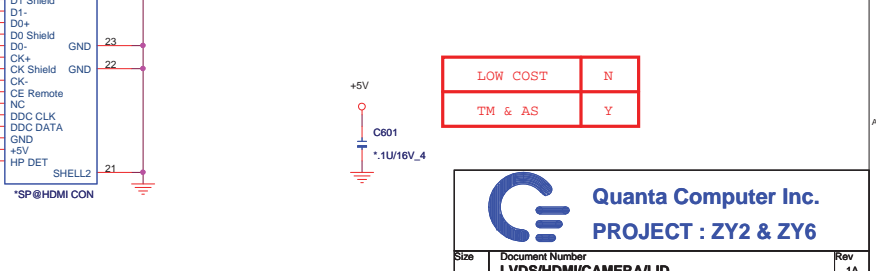
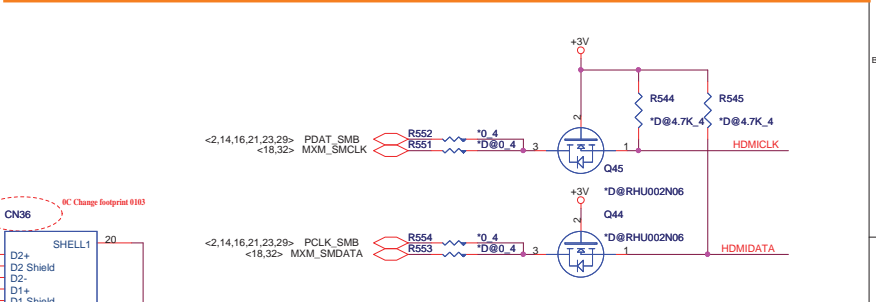
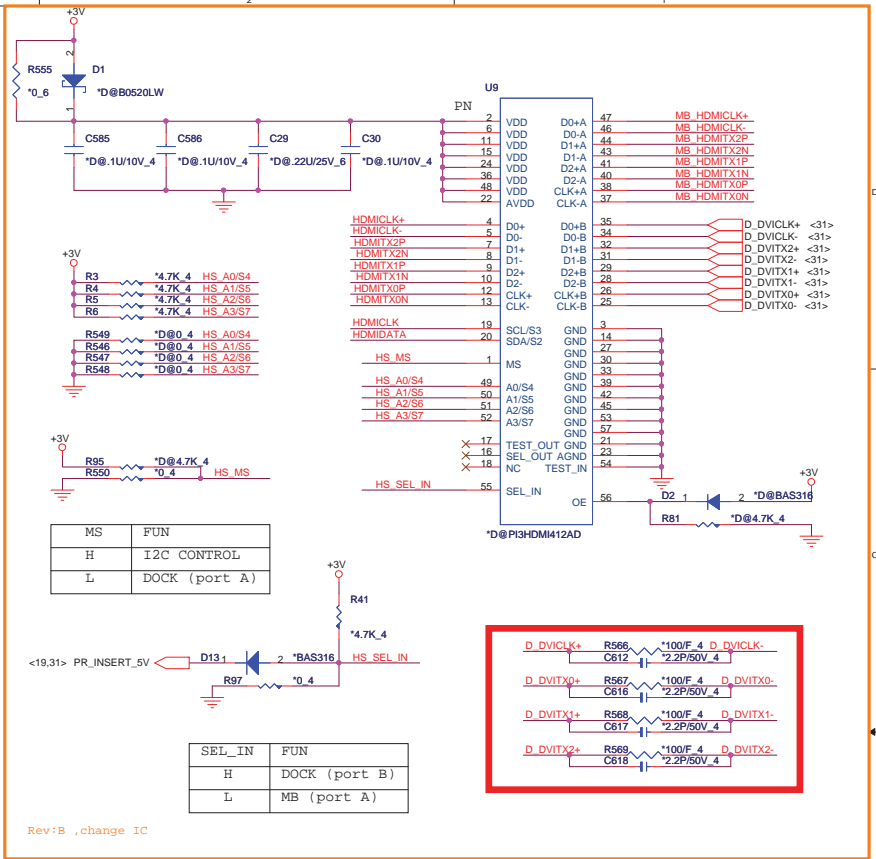
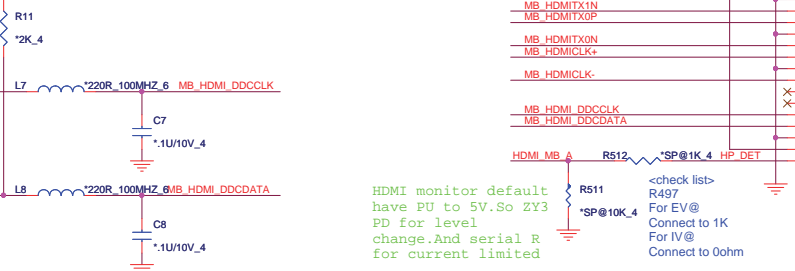
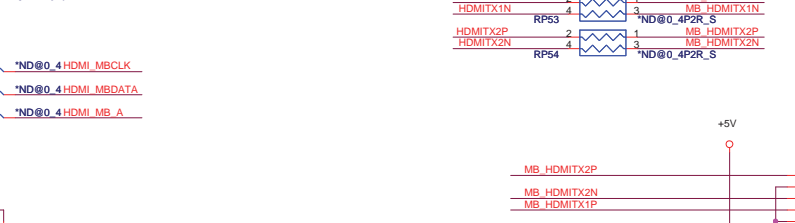
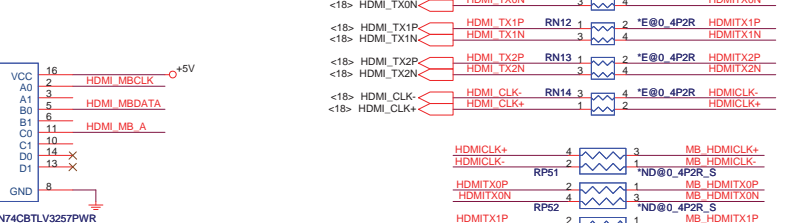
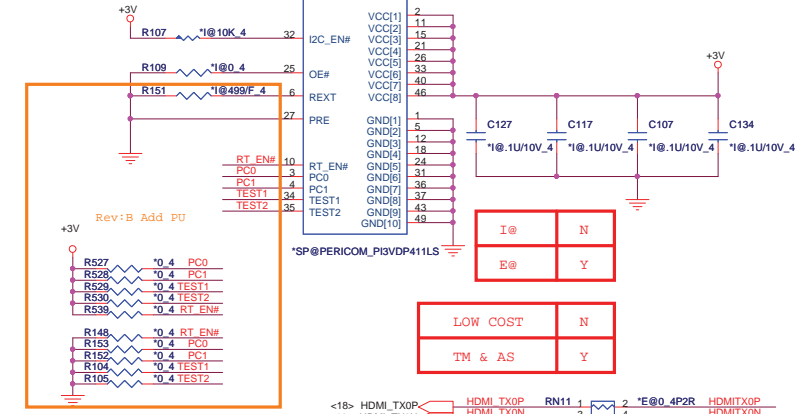
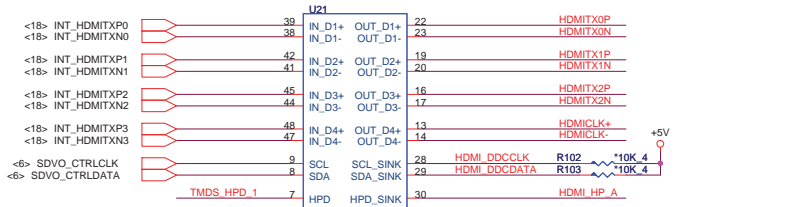


Backlight Control

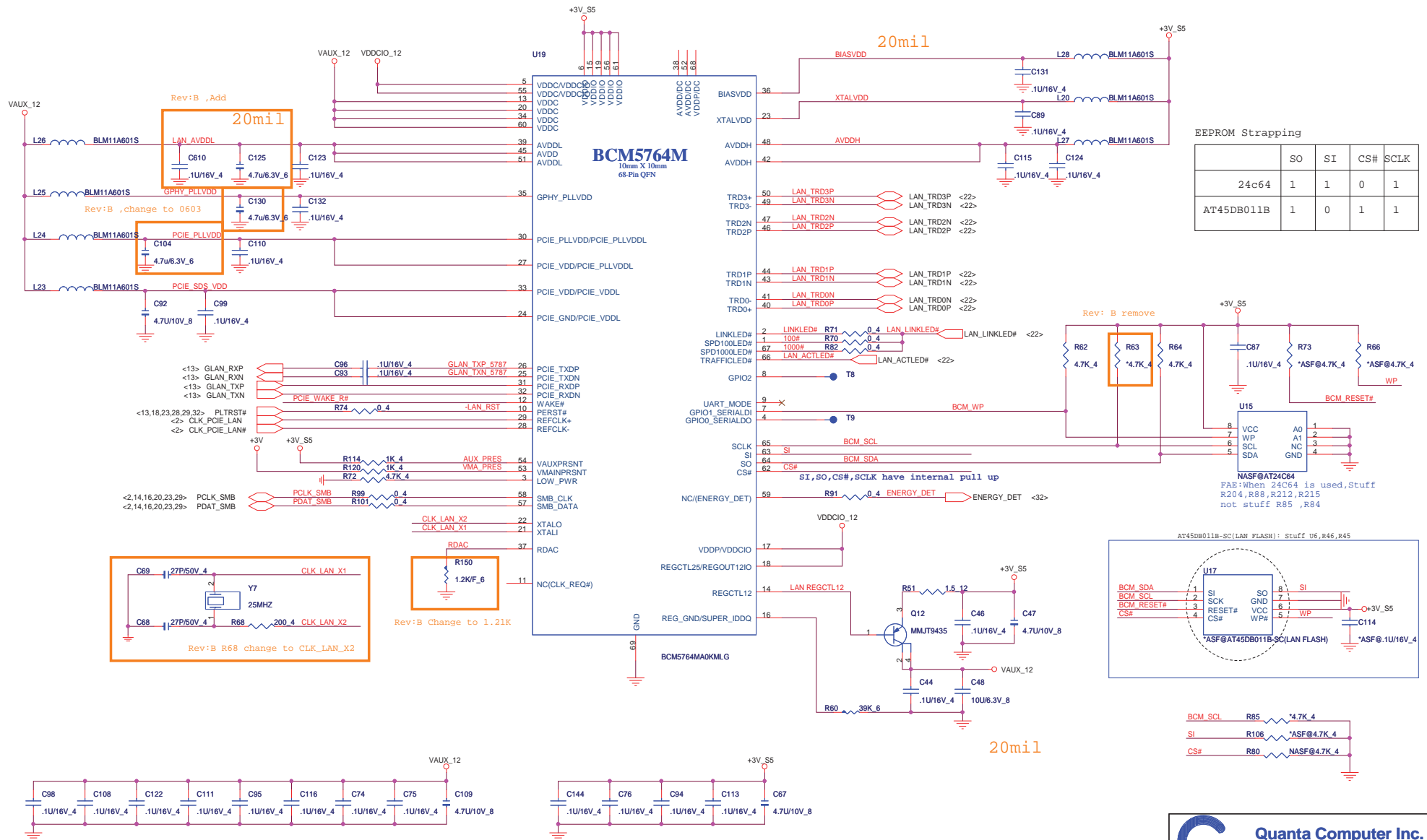
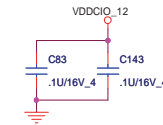
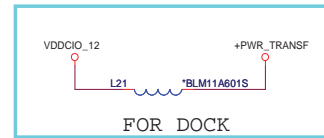
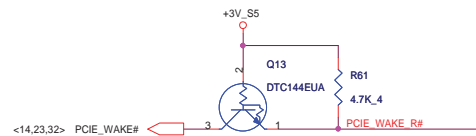


DVI-I CONNECTOR (DVI-D)

	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	

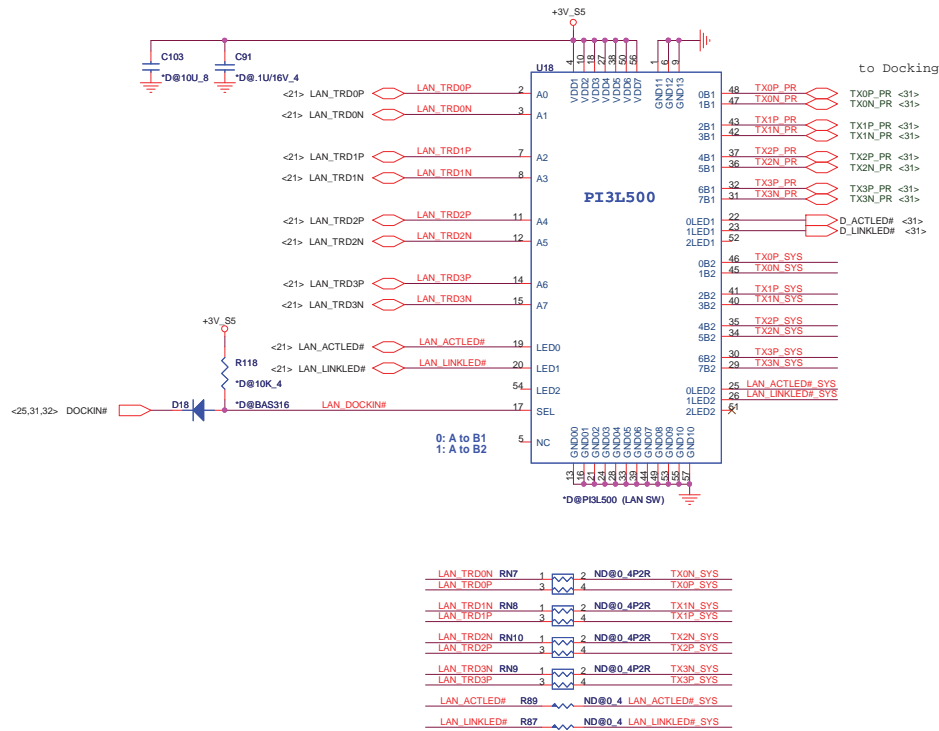


LAN



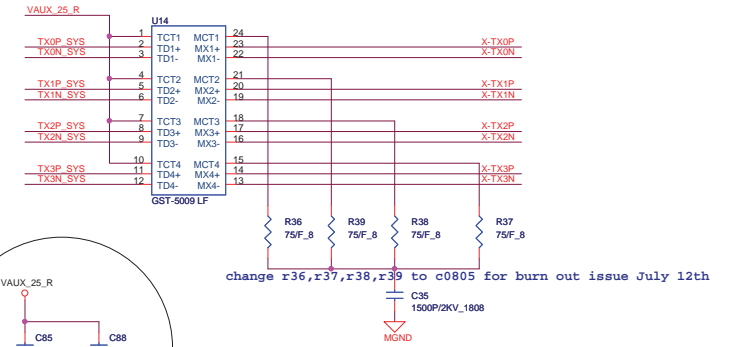
Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset

LAN SWITCH

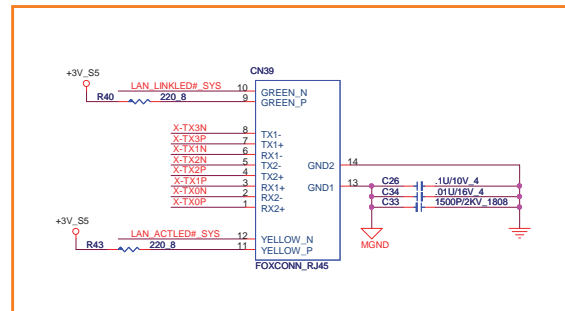


Transformer

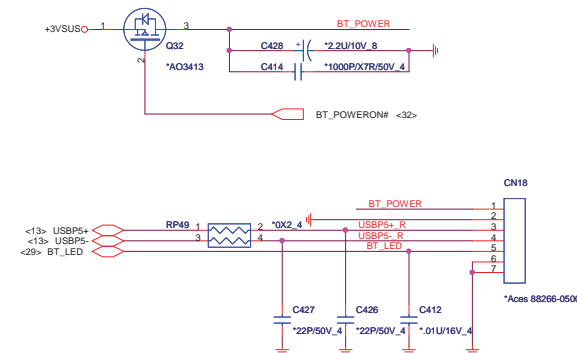
Source 1: DELTA LFE9249 DB0ZR1LAN11
Source 2: Bothand GST5009 DBKN1NLAN03



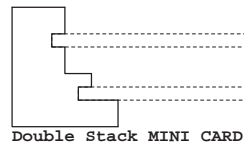
RJ45-11



BLUETOOTH MODULE CONNECTOR



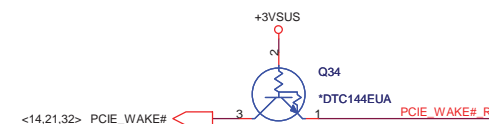
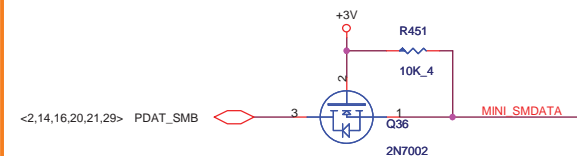
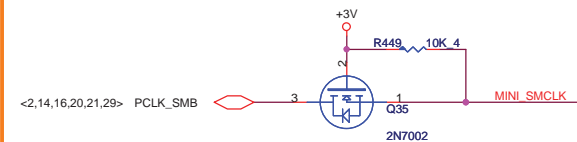
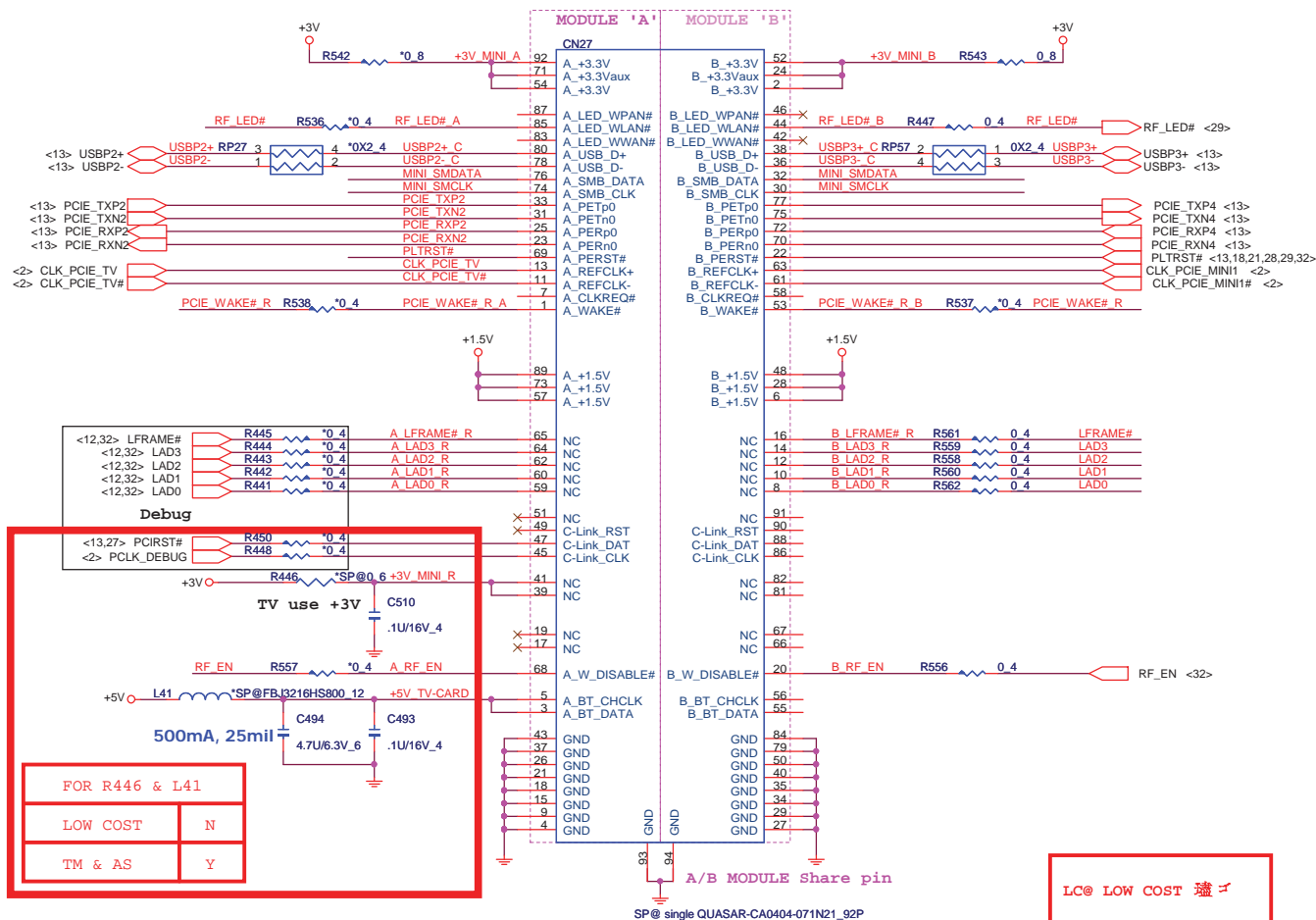
MINI-CARD



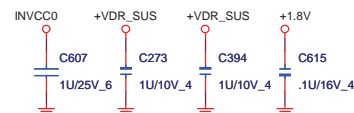
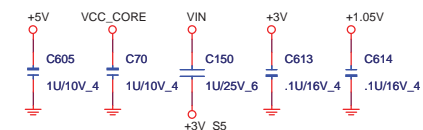
MODULE 'A' TV card

MODULE 'B' Wireless card

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538



FOR EMI



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number MINI PCI-E card/TV/TPM
------	--

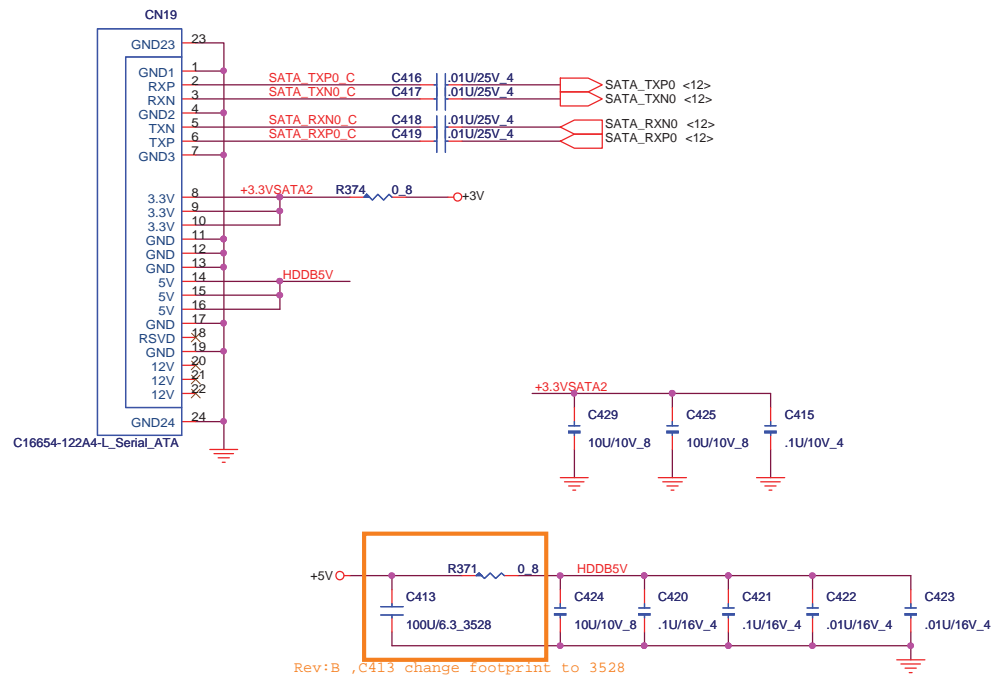
Date: Tuesday, August 12, 2008

Rev
1A

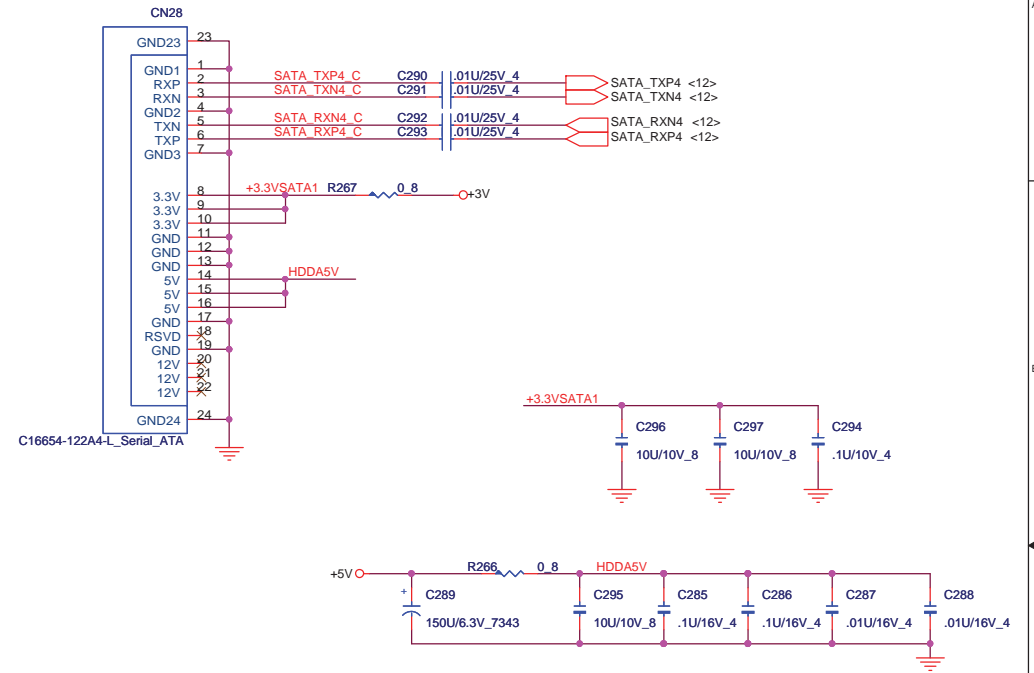
SATA HDD

11/8 REV:B Conn. 奔奕粘 CN28 & CN19

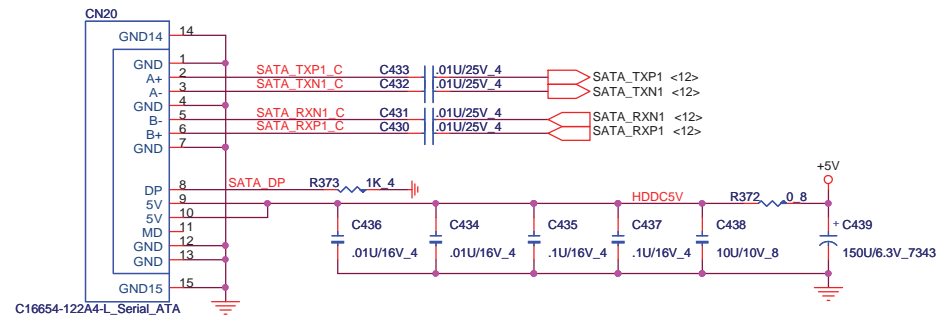
Main




2ND SATA HDD



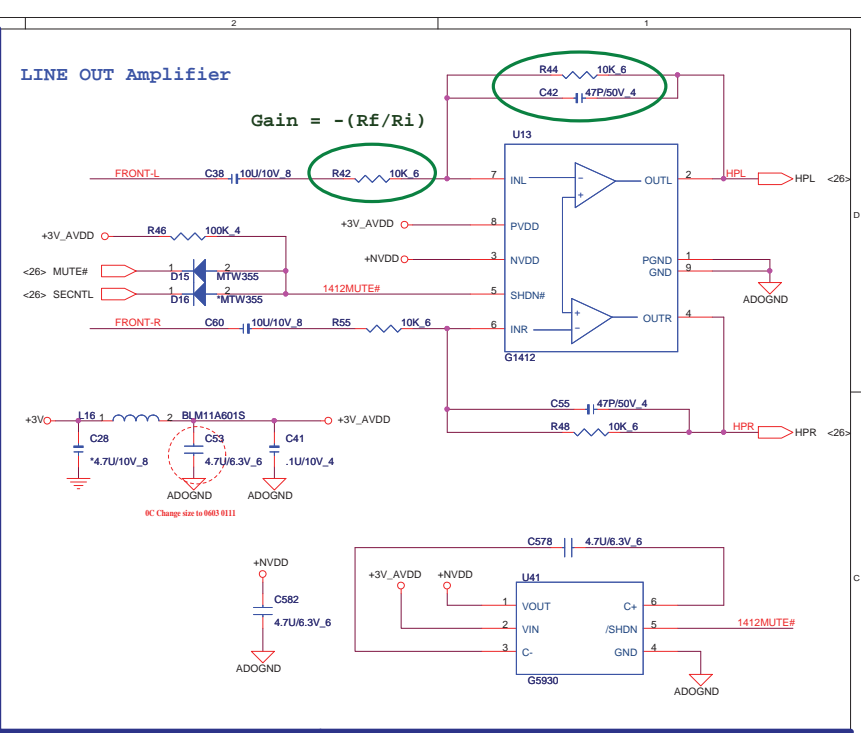
ODD (SATA)



 Quanta Computer Inc. PROJECT : ZY2 & ZY6		Size	Document Number	Rev
		SATA-HDD & ODD		1A
Date:	Wednesday, August 13, 2008	Sheet	24	of 40

[illegible]

[illegible]



TM	N
AS & LOW COST	Y

VR

VR7

<32> DIGVOL_UP → DIGVOL_UP 2

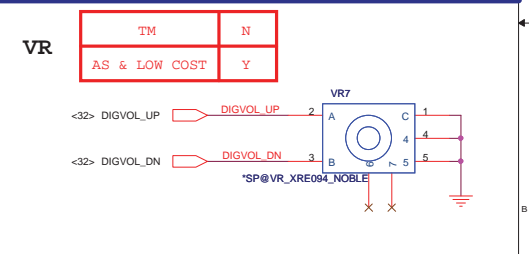
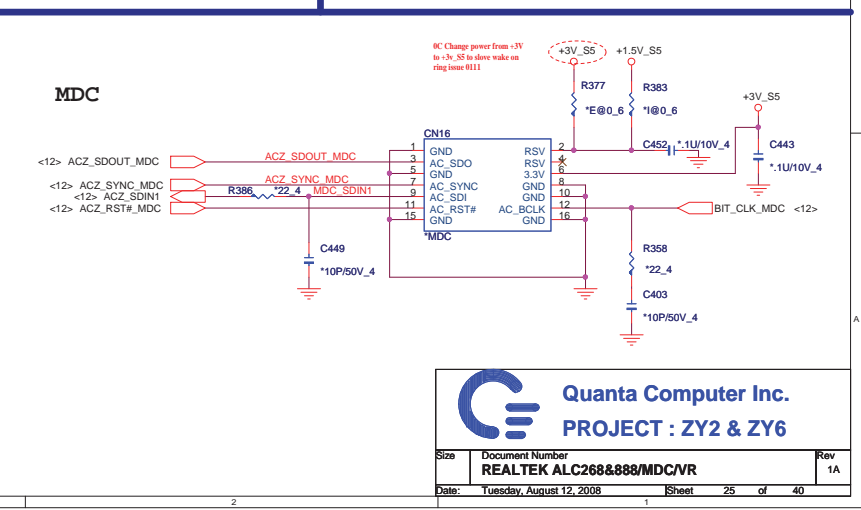
<32> DIGVOL_DN → DIGVOL_DN 3

*SP*VR_XRE094_NOBLE

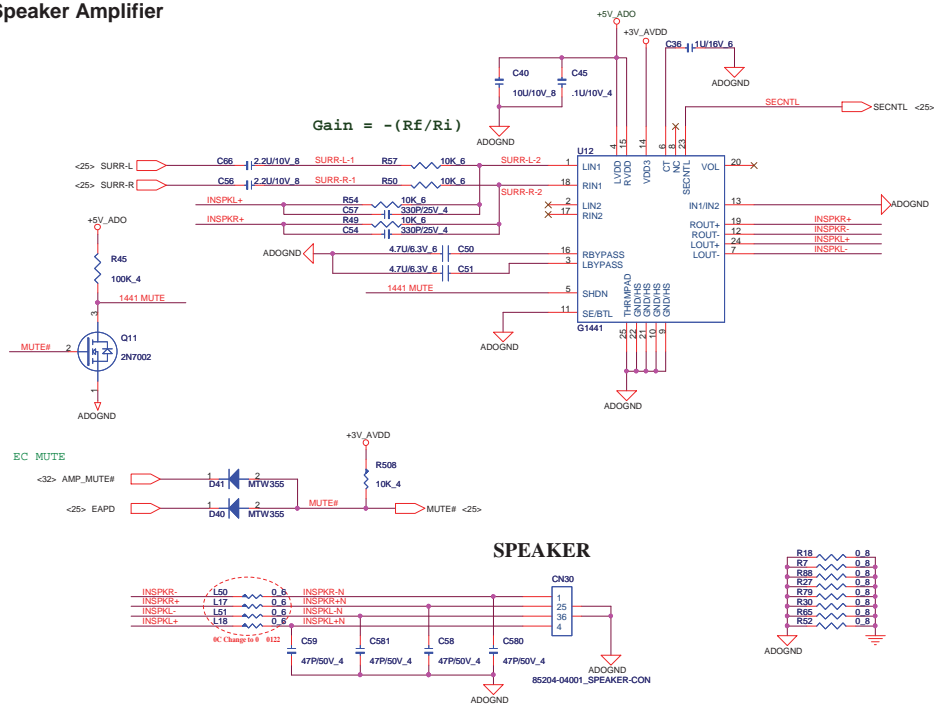
1 4 5 6

X X

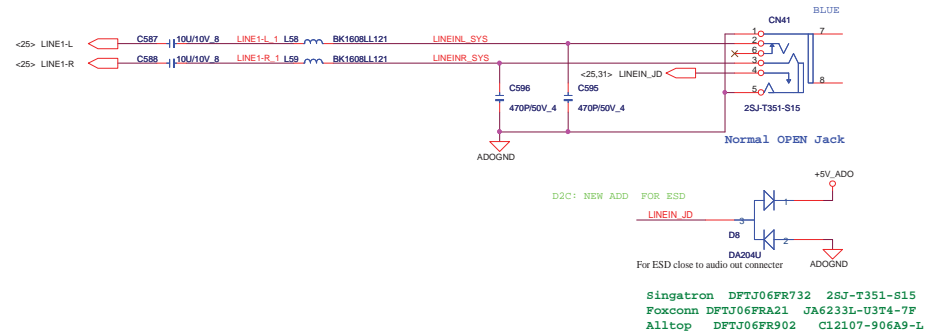
TM	N
AS & LOW COST	Y

[illegible]

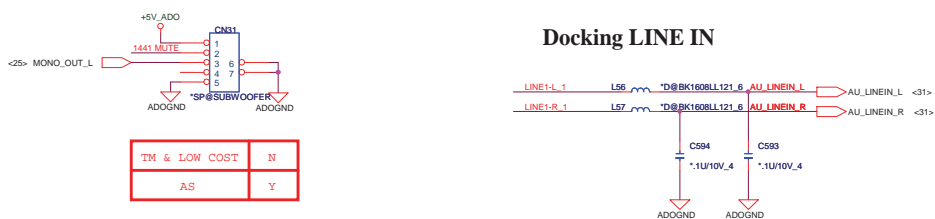
Speaker Amplifier



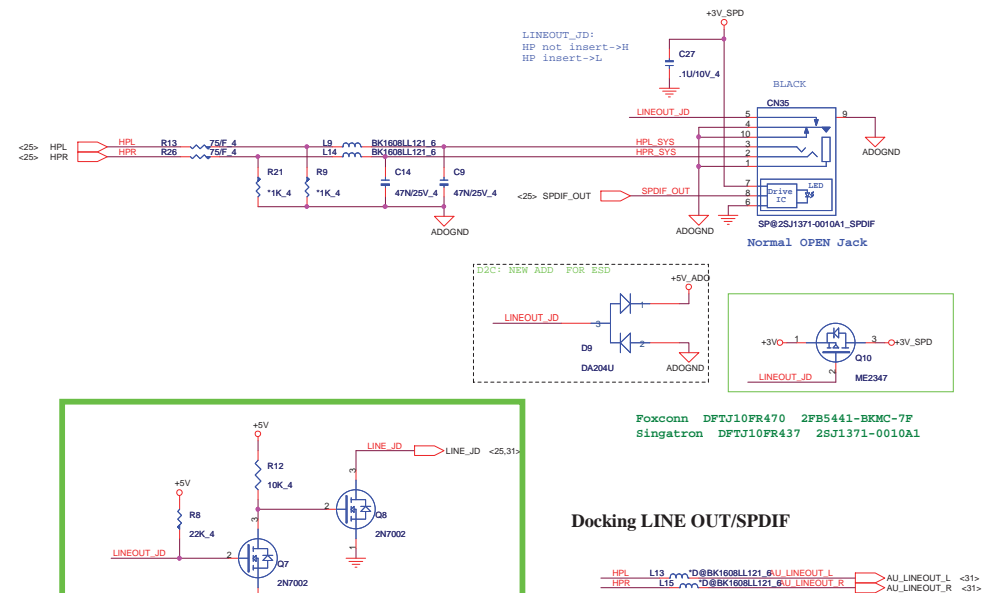
SYSTEM LINE IN/SUBWOOFER



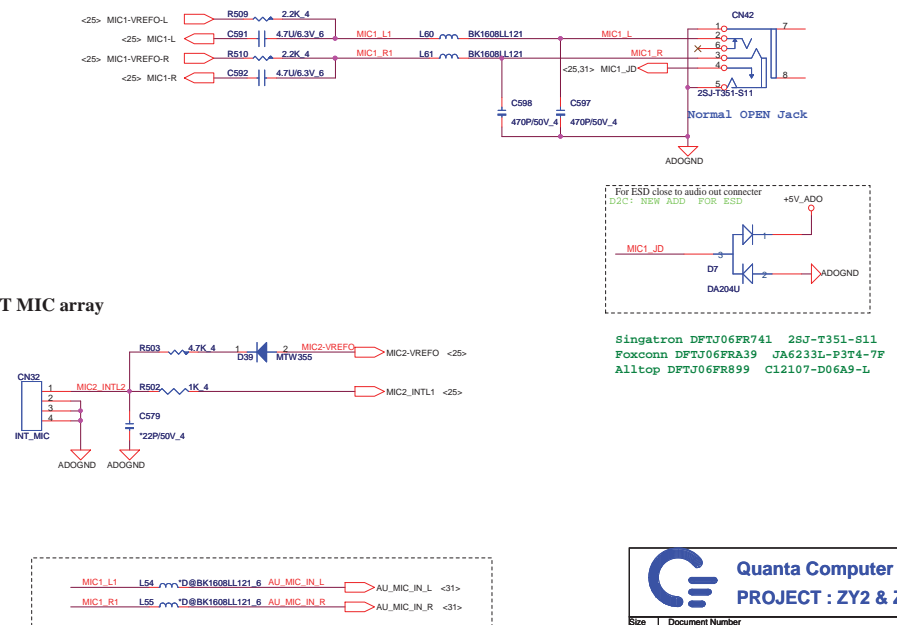
Docking LINE IN

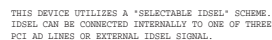


SYSTEM LINE OUT/SPDIF



MIC

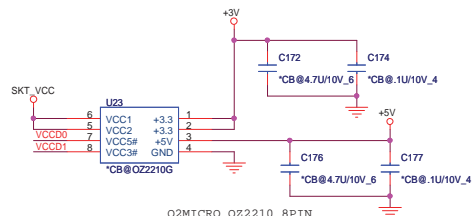
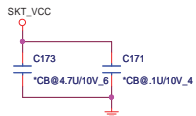
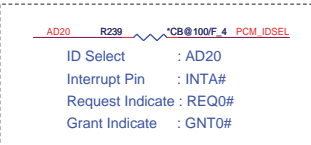




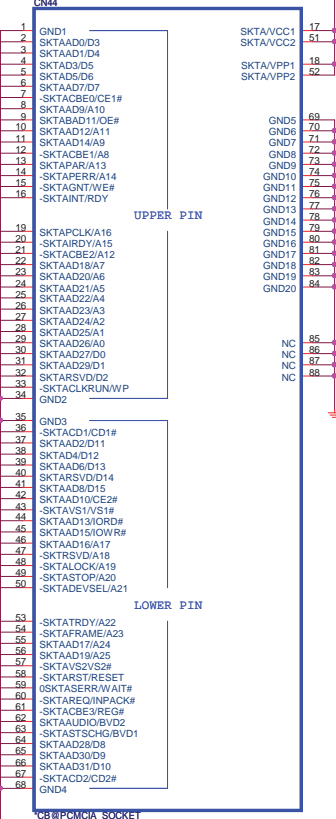
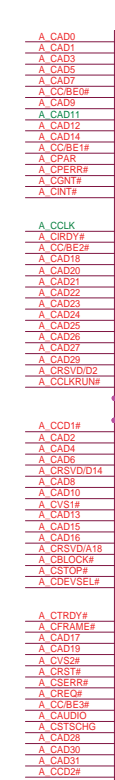
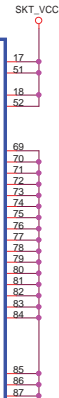
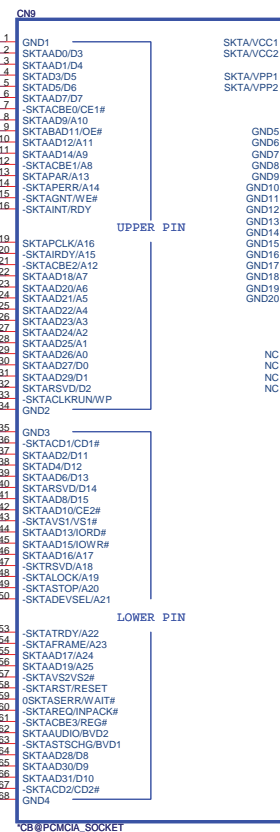
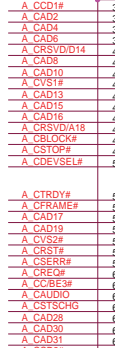
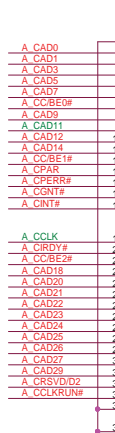
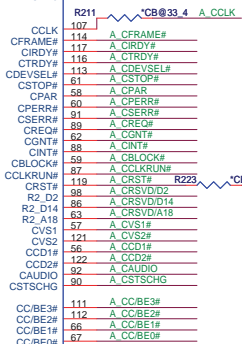
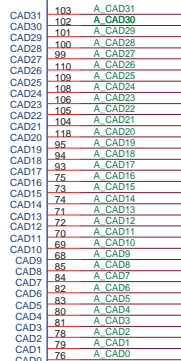
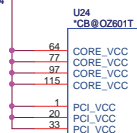
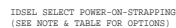
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

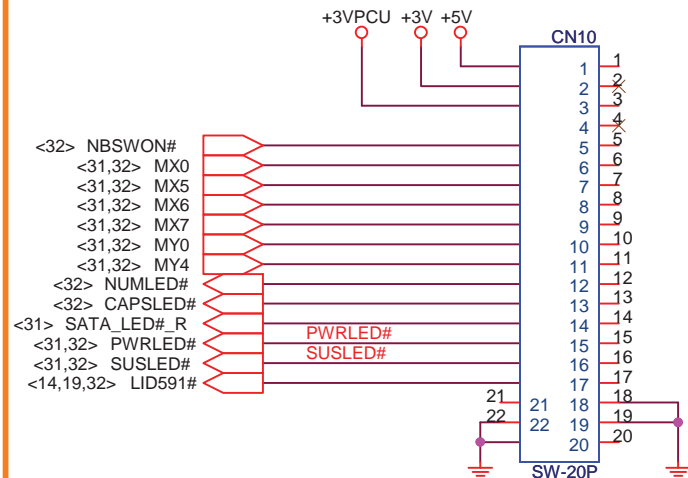


O2MICRO OZ2210 8PIN
SINGLE SLOT PARALLEL
POWER SWITCH

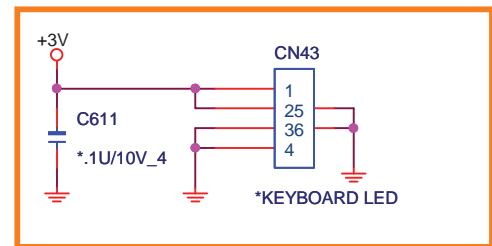
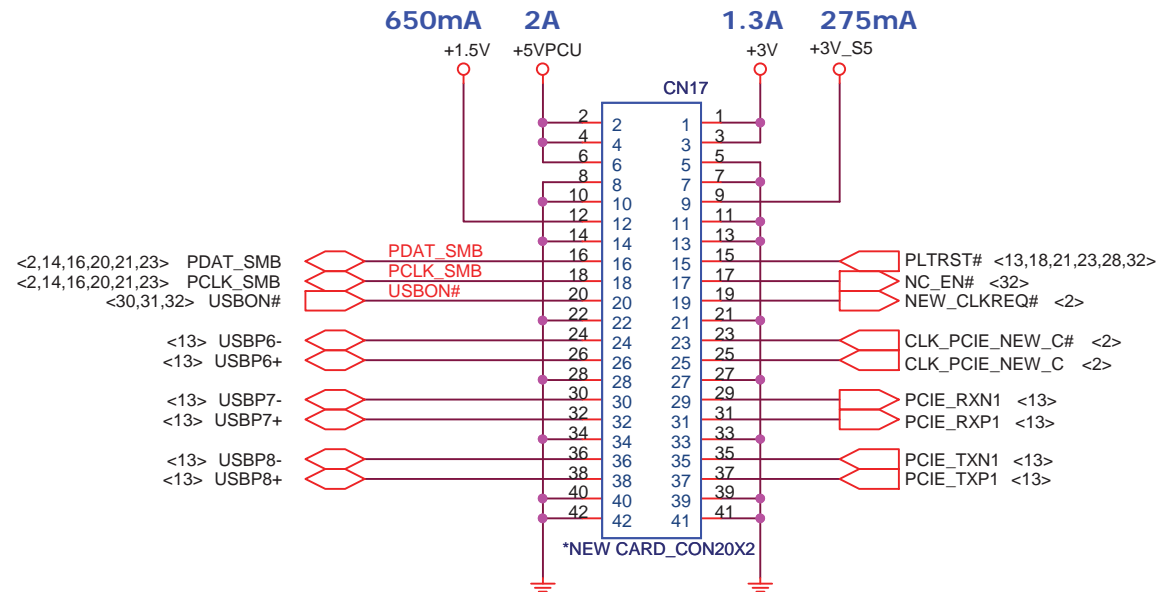
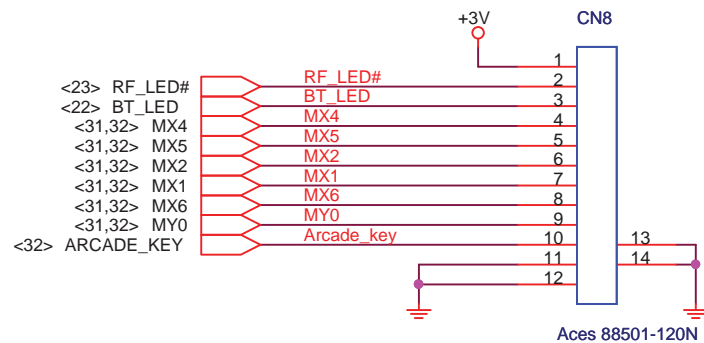


To NEW-CARD & EXT. USB

REV:B, CN10 change footprint



REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Rev:B Add CN43 For backlight KB

Rev:B Change to 蛾 to ↓PAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395

Fncion	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4

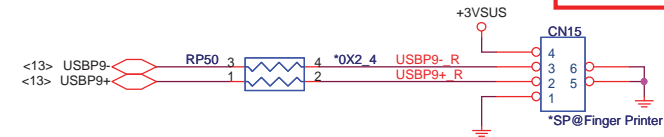


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

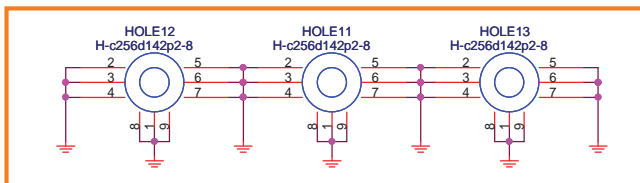
Size	Document Number	Rev
	BTB CONN.	1A
Date:	Tuesday, August 12, 2008	Sheet 29 of 40

Finger Printer

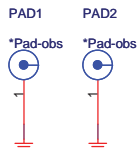
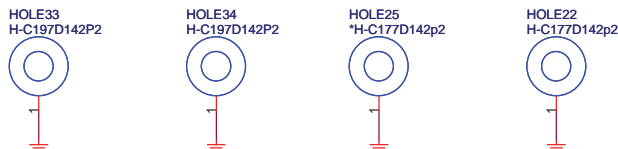
TM & AS	Y
LOW COST	N



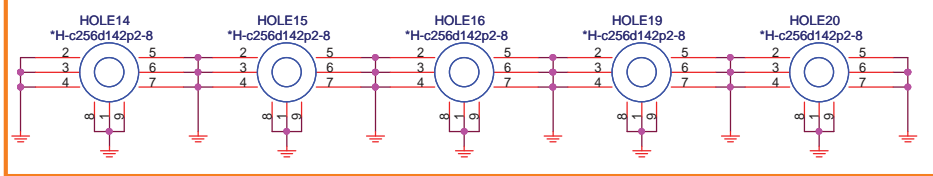
HOLES CPU NUT (BOT)



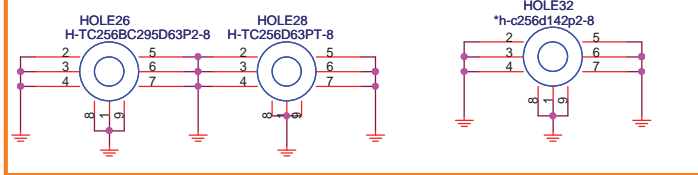
Rev : B Add MINI NUT



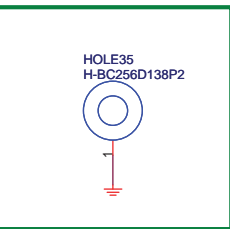
MXM NUT (BOT)



MDC NUT (TOP)

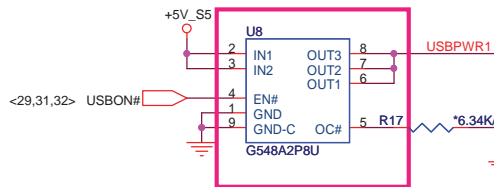


Rev:B New add HOLE32
HOLE26 & 28 Change footprint

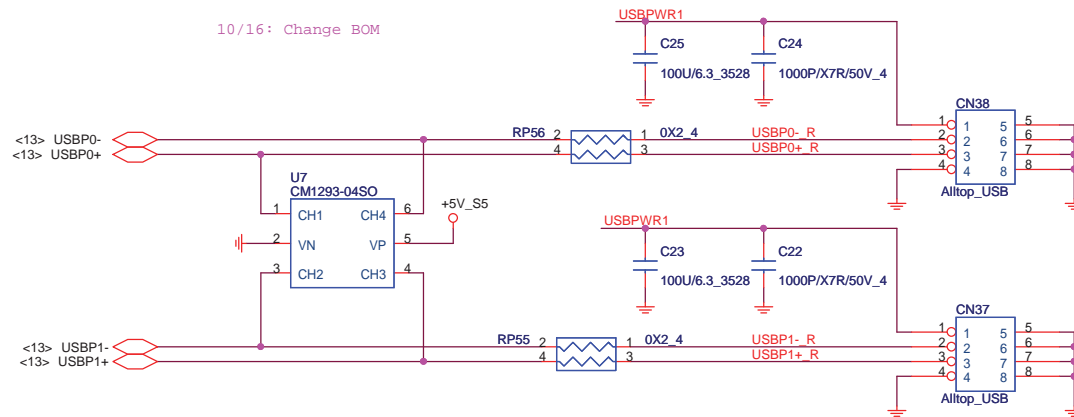


HOLE35 璫槐 BOT

USB

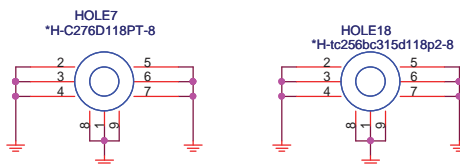
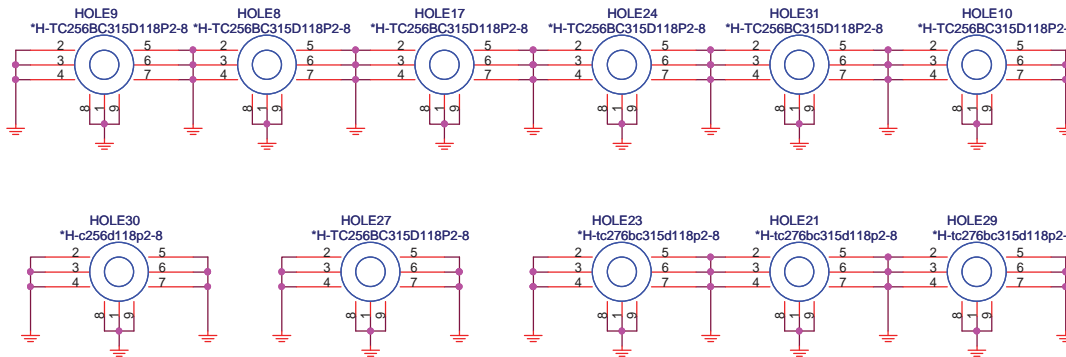


10/16: Change BOM



USBP0- R	D47	2	1	MLVG06031R
USBP0+ R	D48	2	1	MLVG06031R
USBP1- R	D49	2	1	MLVG06031R
USBP1+ R	D50	2	1	MLVG06031R

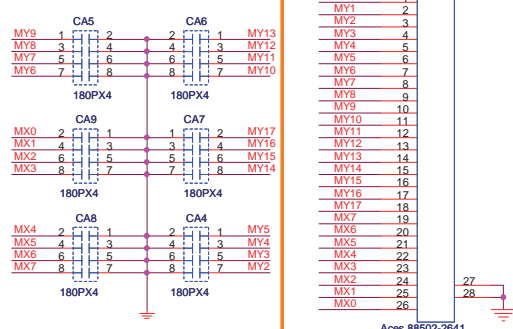
REV:C Modify



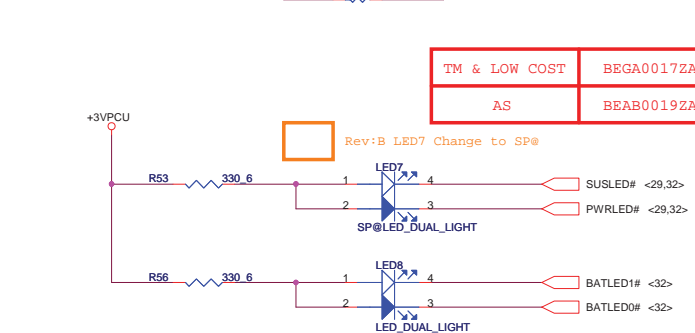
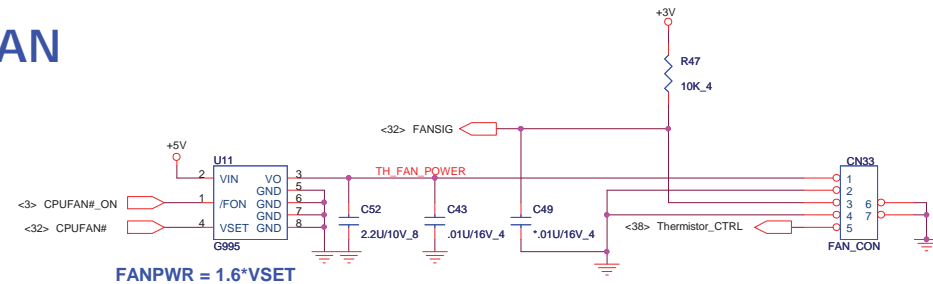
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	USB/FINGER PRINTER	1A
Date:	Tuesday, August 12, 2008	Sheet 30 of 40

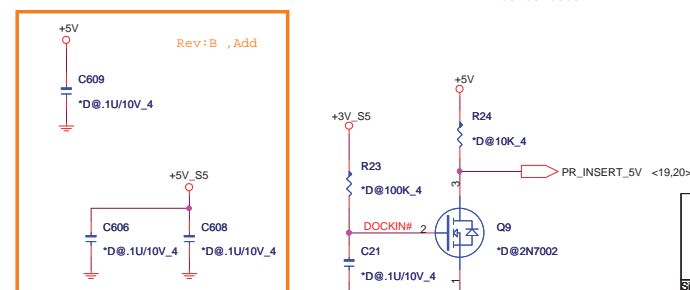
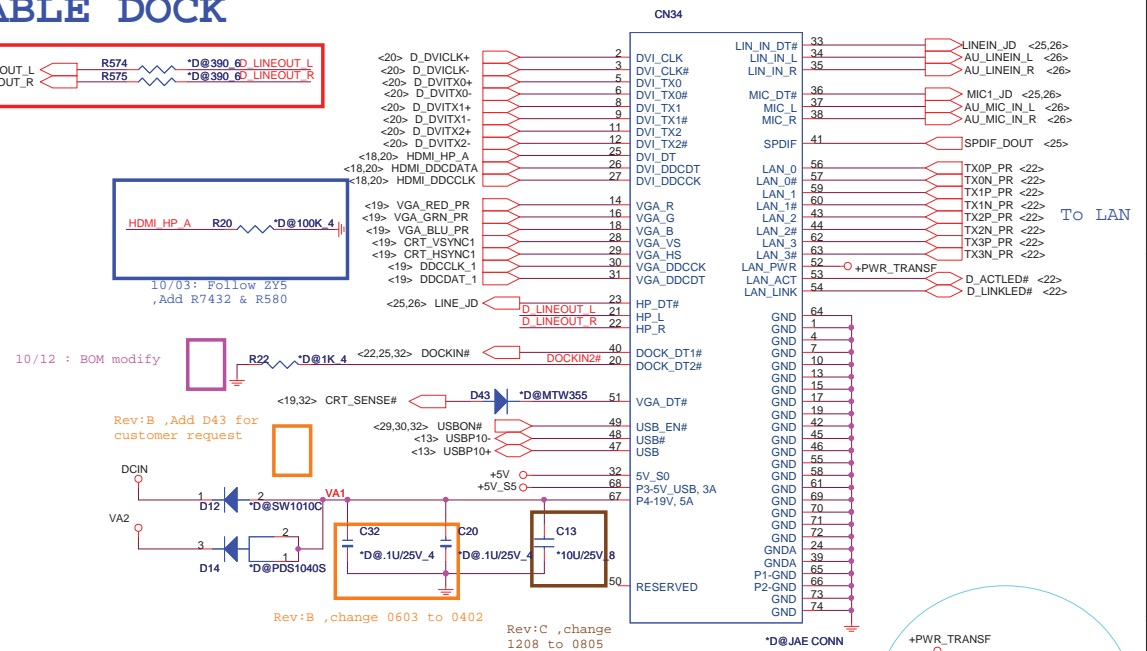
<32>	MY14	MY15
<32>	MY15	MY14
<32>	MY13	MY13
<32>	MY12	MY12
<32>	MY12	MY11
<32>	MY11	MY10
<32>	MY10	MY9
<32>	MY9	MY8
<32>	MY8	MY8
<32>	MY7	MY7
<32>	MY6	MY6
<32>	MY6	MY5
<32>	MY5	MY4
<29,32>	MY4	MY3
<32>	MY3	MY3
<29,32>	MY3	MY2
<29,32>	MY2	MY2
<29,32>	MY2	MY1
<29,32>	MY1	MY1
<32>	MY1	MY0
<29,32>	MY0	MY0
<29,32>	MY0	MX1
<32>	MY16	MY16
<32>	MY17	MY17

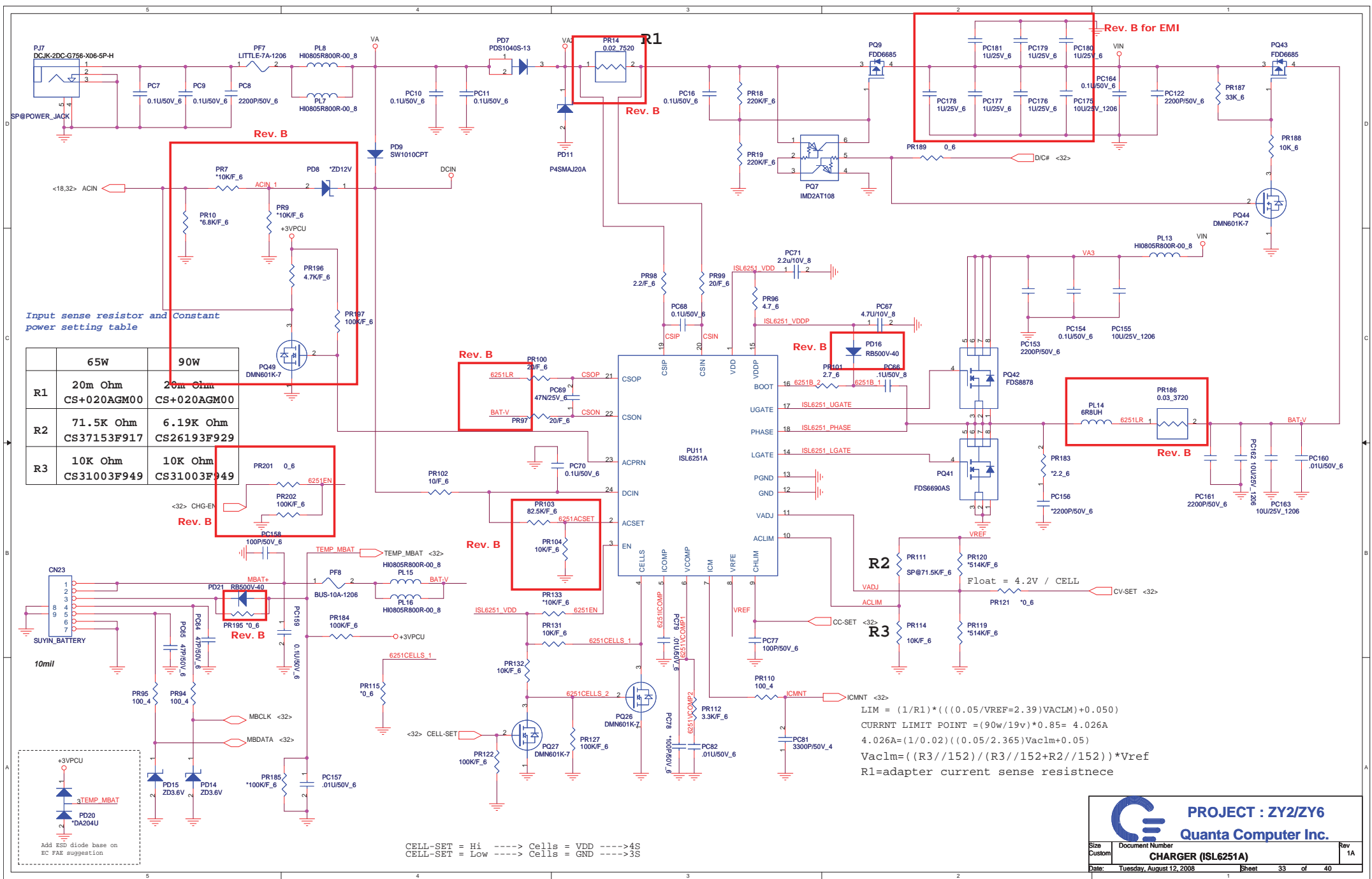


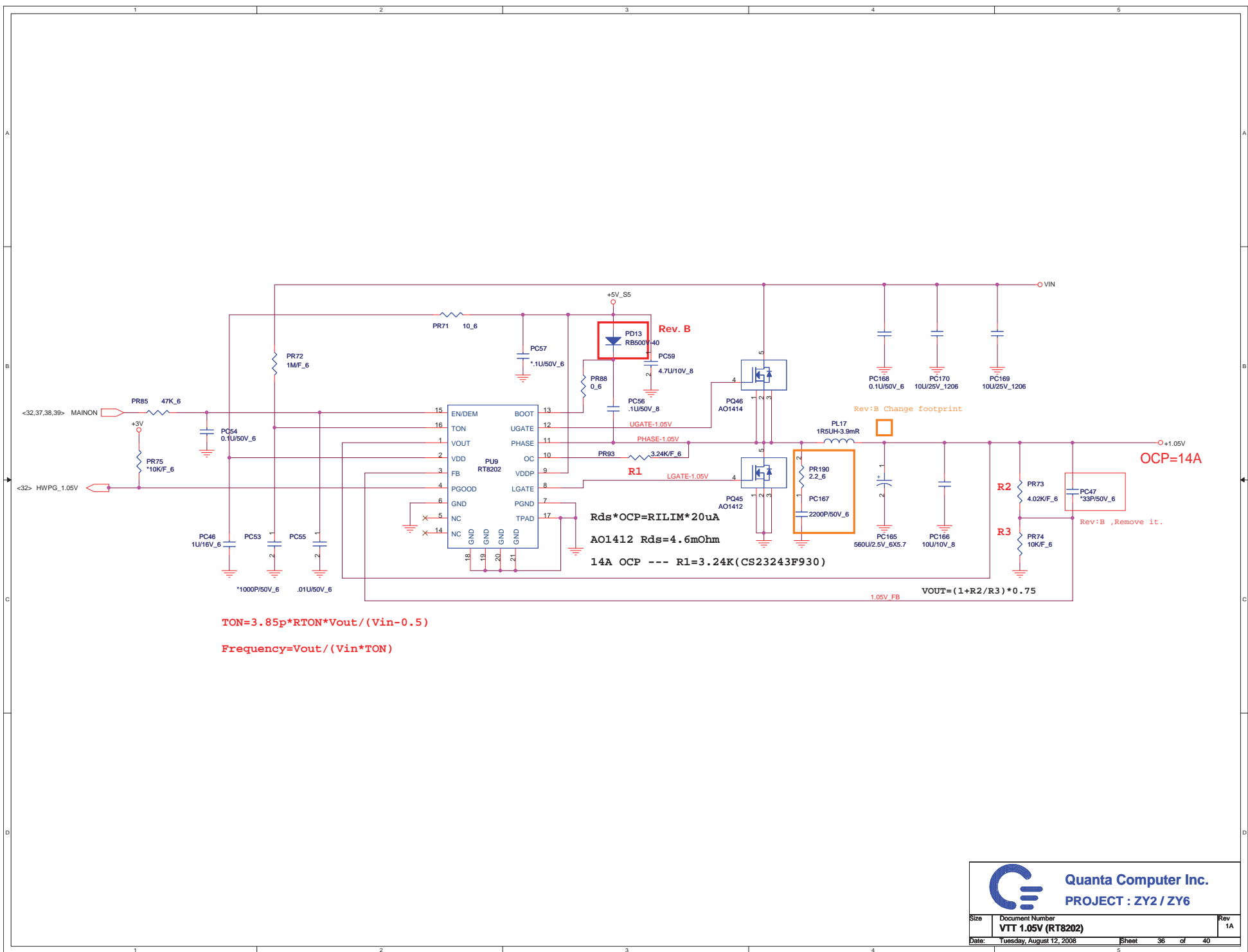
+5V
C37
2.2U/10V_8



Schematic diagram of the audio output stage. It shows two input lines, AU_LINEOUT_L and AU_LINEOUT_R, connected to resistors R574 and R575 respectively. These resistors are connected to a common node that branches into two output lines: LINEOUT_L and LINEOUT_R. The output lines are labeled with 'D@390 6'.



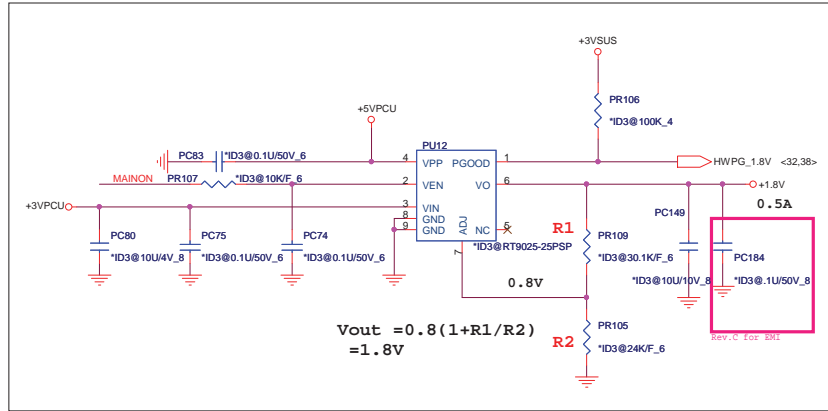




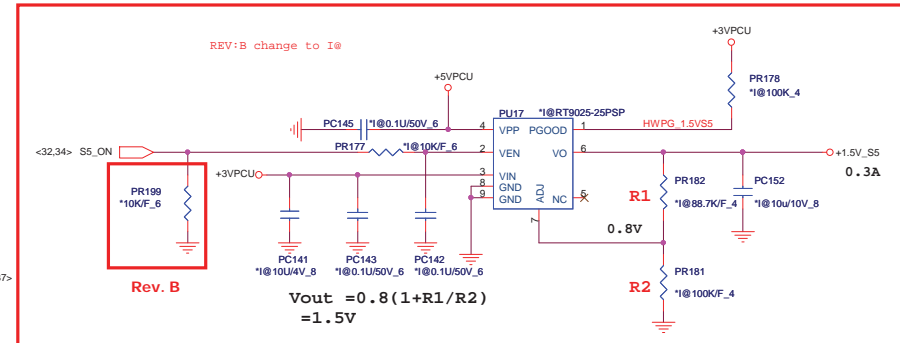
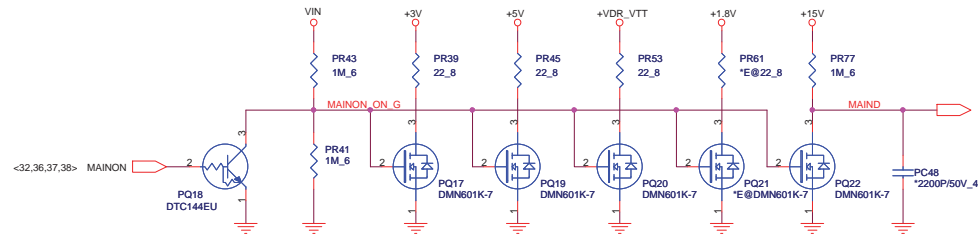
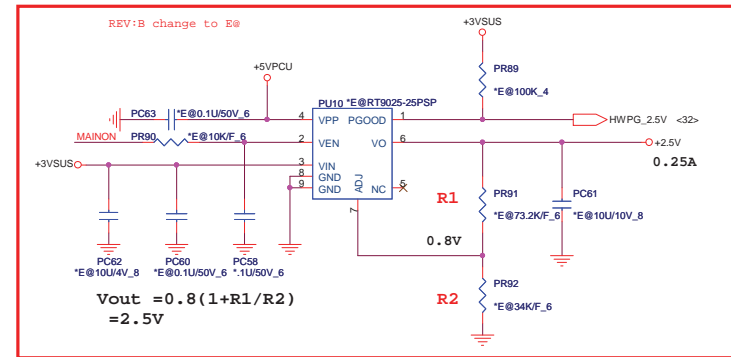
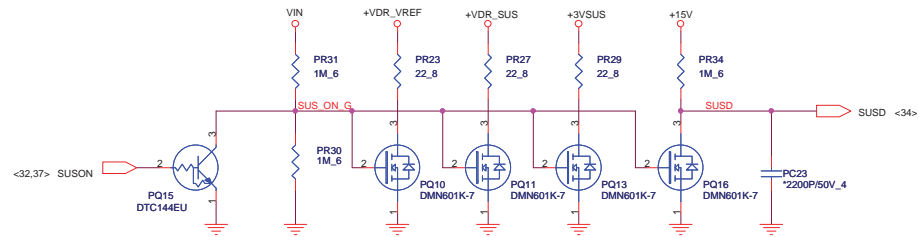
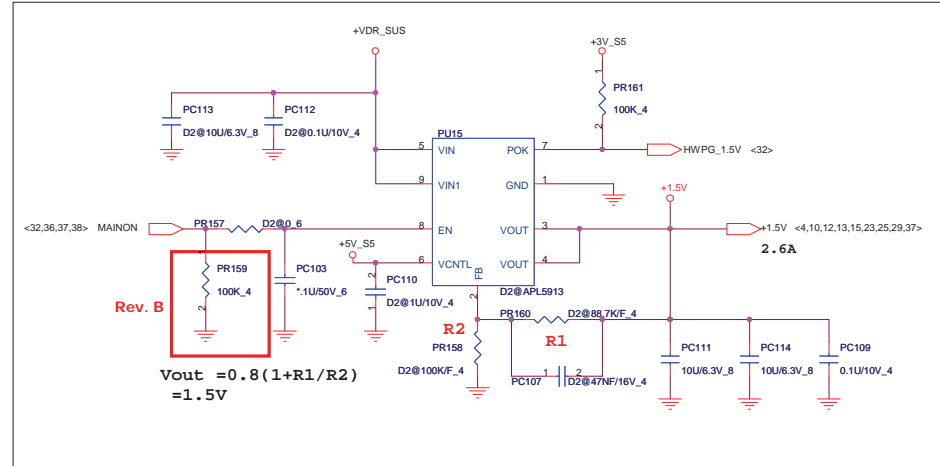
Quanta Computer Inc.
PROJECT : ZY2 / ZY6

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	VTT 1.05V (RT8202)	1A
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for DDR3 and UMA

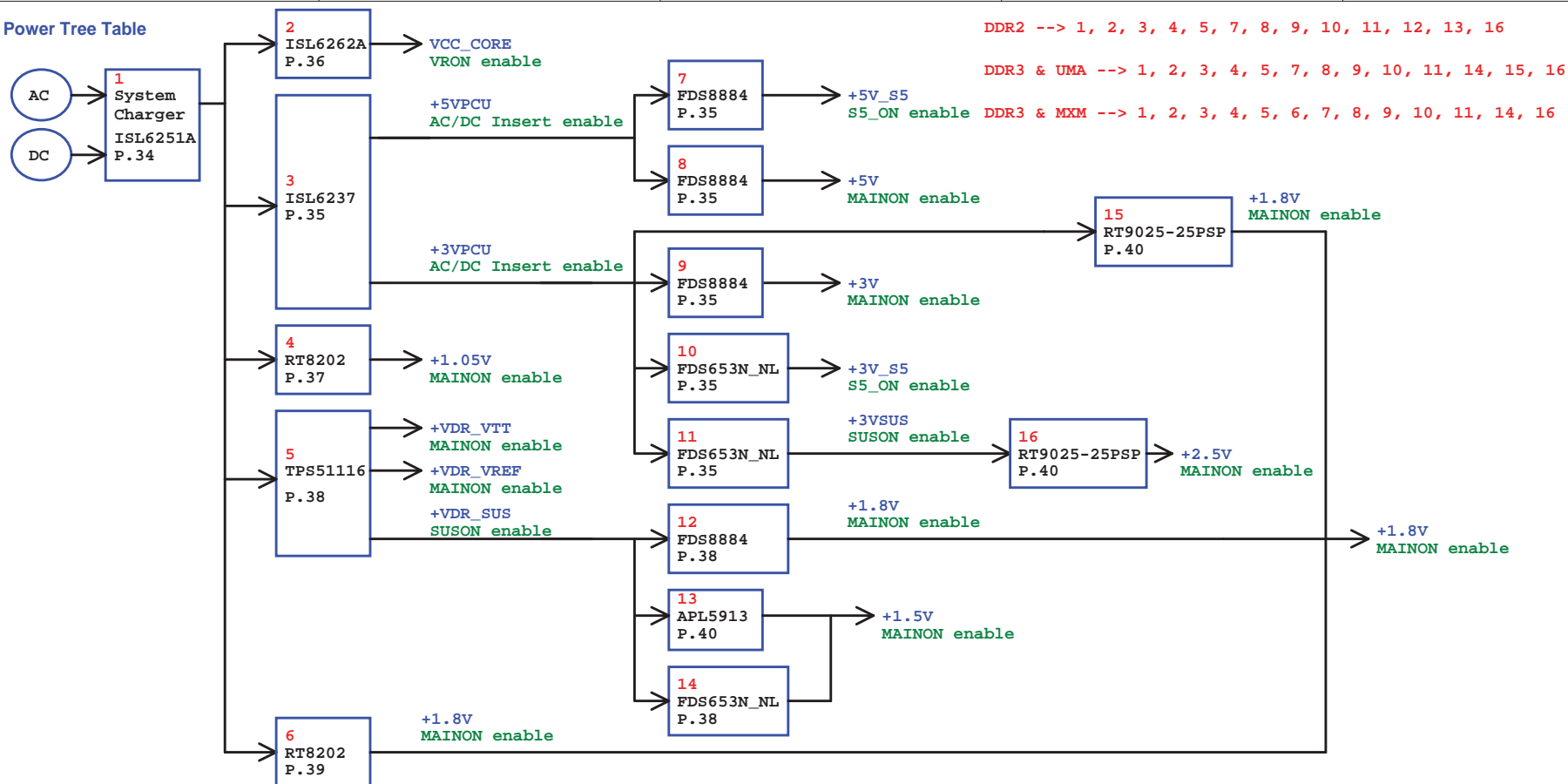


DDR3 -- NC



REV:B change to E@

Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T)
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Model				REV		CHANGE LIST		MODEL	ZY2		
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)							X	1A	
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : Add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)							X	1A	
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
										1A	2A
								2A	Page19 : change U22 LVDS PWR SW IC to TI for display issue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 : Change U13 packing from TQFN to TDFN for vendor request		
			1A	2A							
			1A	2A							
			1A	2A							
			1A	2A							
			1A	2A							
	2B	Page20 : Add R566 ,R567 ,R568 ,R569 ,C612 ,C616 ,C617 ,C618 solve the HDMI EMI issue. Page26 : Change CN41 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Change CN42 PIN 7 & 8 from ADOGND to NC solve the ESD issue. Page30 : Add D47 ,D48, D49 & D50 solve the USB ESD issue. Page31 : Add R574 & R575 (390)solve Docking audio noise issue. Page32 : Add EMI resistor (R565) in SPI flash interface.								1A	2A
										1A	2A
										1A	2A
										2A	2B
										2A	2B
										2A	2B
										2A	2B
										2A	2B
										2A	2B
										2B	3A
										2B	3A
										2B	3A
										2B	3A
										2B	3A
	</										